

Compal Confidential

A4WAD MB Schematic Document

LA-C871P

Rev: 1.0

2015.07.13

DAX

Part Number	Description
DA6001ED010	PCB 1DS LA-C871P REV1 MB 1

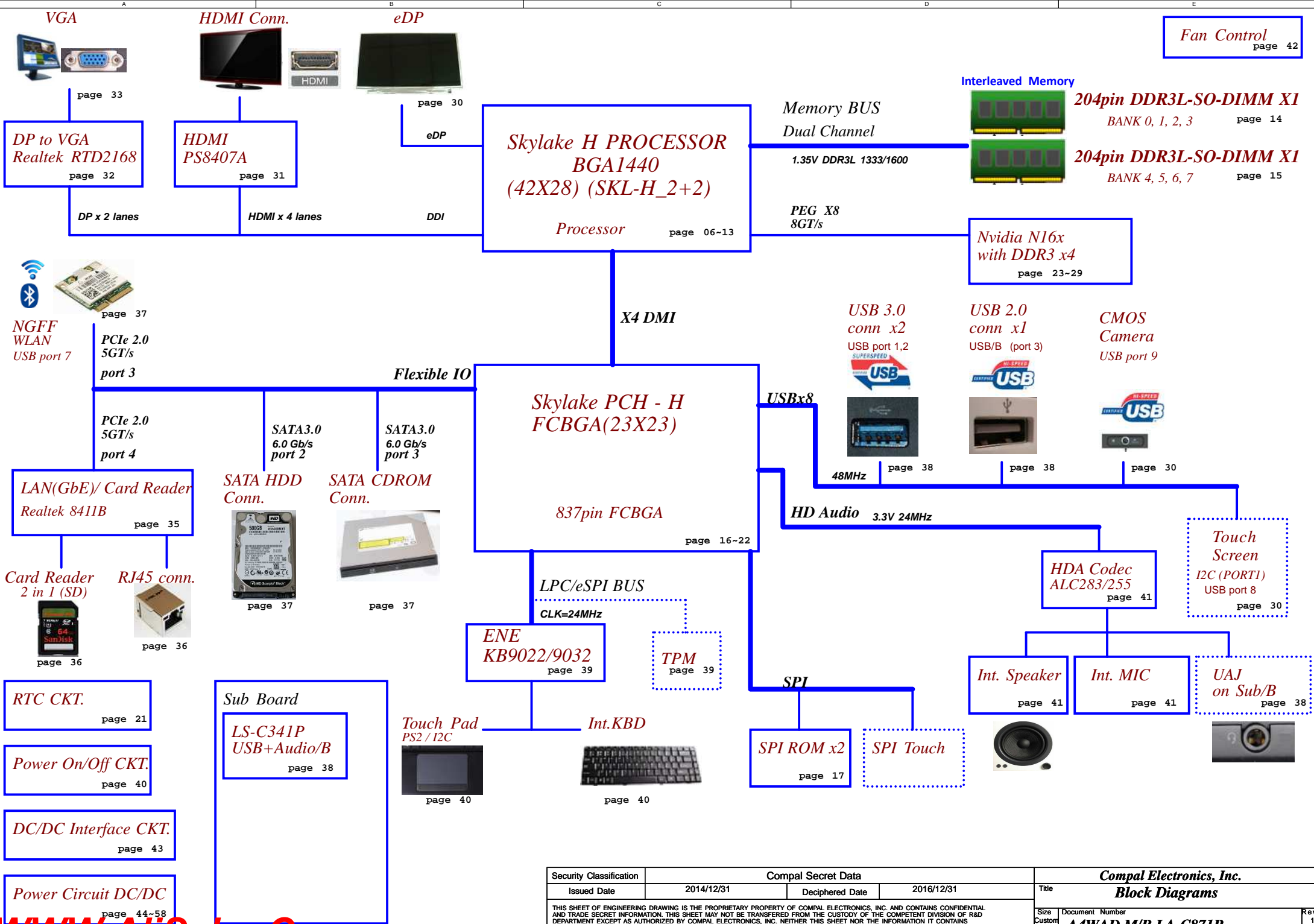
A4WAD_PCB_REV10
PCB@

DAZ

Part Number	Description
DAZ1DS00100	PCB A4WAD LA-C871P LS-C341P

A4WAD_PCB_Panelization
@

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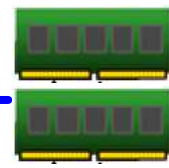
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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V _{BD} min	V _{BD} typ	V _{BD} max	EC AD3
0	0	0 V	0 V	0.300 V	0x00 - 0x0B
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x0C - 0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C - 0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64

BOM Structure Table

BOM Option Table		BOM Option Table	
Item	BOM Structure	Item	BOM Structure
Unpop	@	dGPU	VGA@
Connector	CONN@	N16S-GT	SGT@
EMC requirement	EMC@	N16V-GM	VGM@
EMC requirement depop	@EMC@	Non GPU CG6 funct i on	NGC6@
CODEC(ALC255)	255@	GPU CG6 funct i on	GC6@
CODEC(ALC283)	283@	VRAM BOM Select	X76@
SPI ROM 8M*2	8M_DUAL@	DMIC*1	DMIC@
SPI ROM 8M*1	8M_SINGLE@	For Acer IOAC	IOAC@
UMA only	UMA@	No Acer IOAC	NIOAC@
TPM	TPM@		
CMC	CMC@		
Keyboard backlight	KB@		
LPC MODE for EC	LPC@		
ESPI MODE for EC	ESPI@		
BA Serial	BA@		

I2C Address Table (TBC)

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Touch Panel	reserved		
I2C_1 (+3VS)	TM-P2969-001 (Touch Pad)	0x2C		
	SB8787-1200 (Touch Pad)	0x15		
PCH_SMBCLK (+3VALW)	DIMM1	0xA0		
	DIMM2	0xA4		
	LIS3DHTR(G-sensor)	0x30		
PCH_SML1CLK (+3VALW)	N16S-GT (VGA)	0x9E		
	RTD2168 (CRT)	reserved		
	EC			
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

43 level BOM table

43 Level	Description	BOM Structure
4319YYBOL01	SMT MB AC871 A4WAD QHR7 1.6G UMA HDMI	QHR7@/1dMIC@/255@/8M_SINGLE@/BA@/EMC@/IOAC@/KB@/LPC@/PCB@/PCH@/TPM@/XDP@/ES@/UMA@
4319YYBOL02	SMT MB AC871 A4WAD QHR7 1.6G GM2G HDMI	QHR7@/1dMIC@/255@/8M_SINGLE@/BA@/EMC@/IOAC@/KB@/LPC@/PCB@/PCH@/TPM@/XDP@/ES@/VGA@/VGM@/NGC6@/X7601@
4319YYBOL03	SMT MB AC871 A4WAD QHPW 2.2G GM2G HDMI	QHPW@/1dMIC@/255@/8M_SINGLE@/BA@/EMC@/IOAC@/KB@/LPC@/PCB@/PCH@/TPM@/XDP@/ES@/VGA@/VGM@/NGC6@/X7601@
4319YYBOL04	SMT MB AC871 A4WAD QHPW 2.2G GT2G HDMI	QHPW@/1dMIC@/255@/8M_SINGLE@/BA@/EMC@/IOAC@/KB@/LPC@/PCB@/PCH@/TPM@/XDP@/ES@/VGA@/SGT@/GC6@/X7603@/

Power State

STATE	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

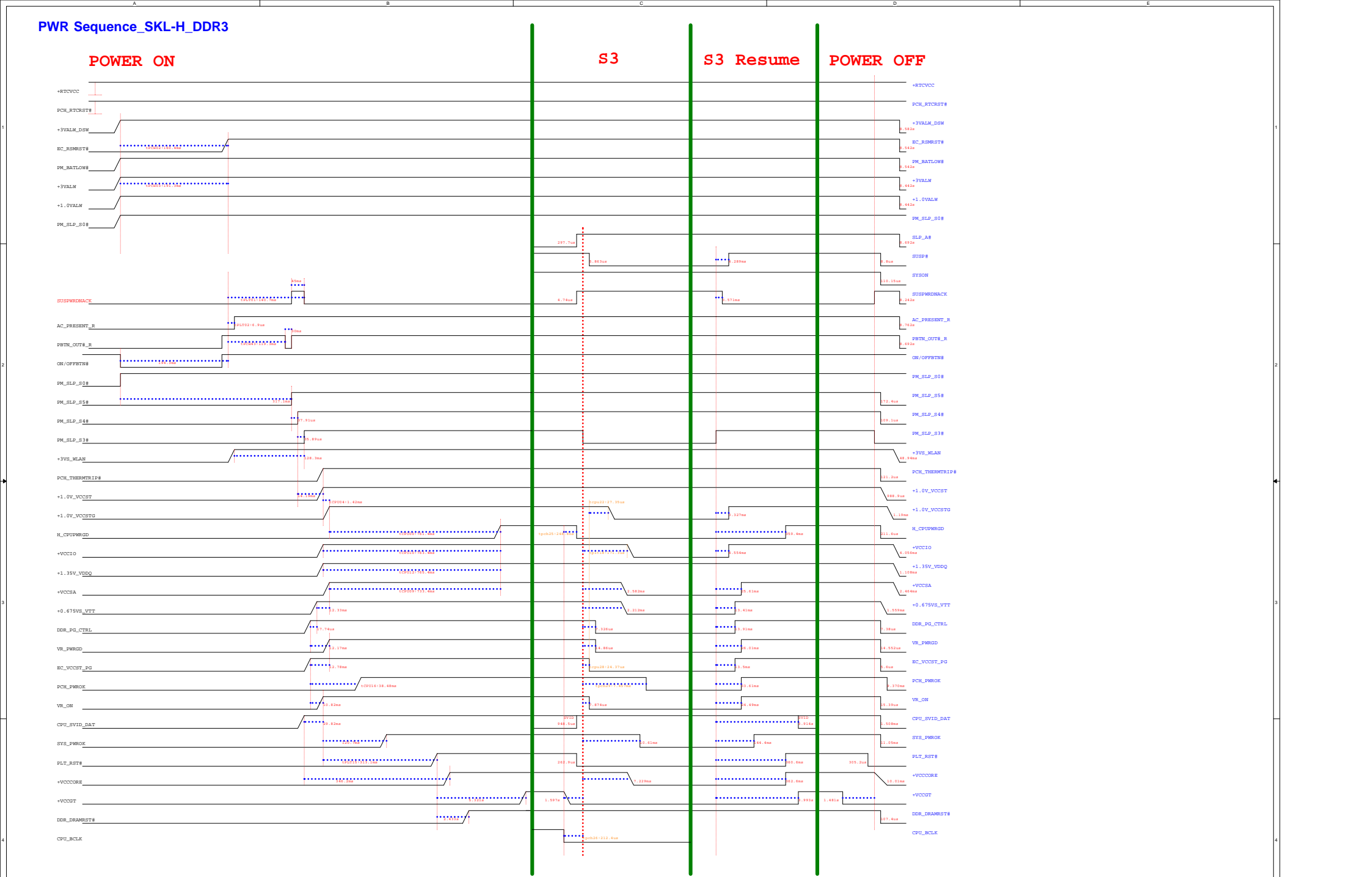
BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	0.7
7	0.8

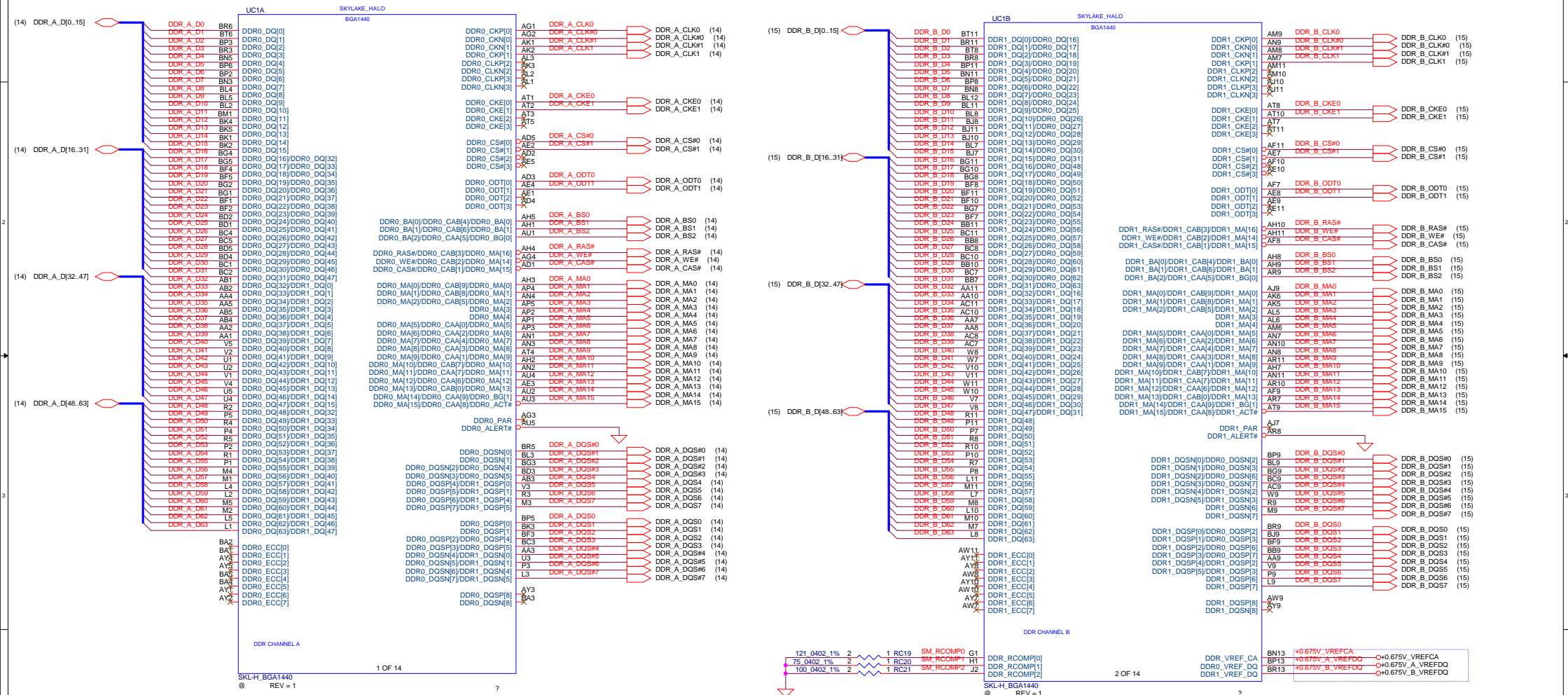
Voltage Rails (TBC)

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
VIN	Adapter power supply	N/A	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+3VALW_PCH	+3VALW power for PCH power rails	ON	ON	ON	ON*
+3VALW_SPI	+3VALW_PRIM supply for the SPI IO	ON	ON	ON	ON
+1.0VALW	+1.0V Always power rail	ON	ON	ON	ON
+1.35V_VDDQ	DDRIII/L-RS +1.35V power rail	ON	ON	OFF	OFF
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.675VS_VTT	DDR +0.675VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+3VSDGPU_AON	+3VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+3VSDGPU_MAIN	+3VS power rail for GPU GC62.0	ON	OFF	OFF	OFF
+VGA_CORE	Core voltage for VGA	ON	OFF	OFF	OFF
+1.8VSDGPU	+1.8VS power rail for GPU	ON	OFF	OFF	OFF
+1.5VSDGPU	+1.5VS power rail for GPU	ON	OFF	OFF	OFF
+1.05VSDGPU	+1.05VS power rail for GPU	ON	OFF	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.					

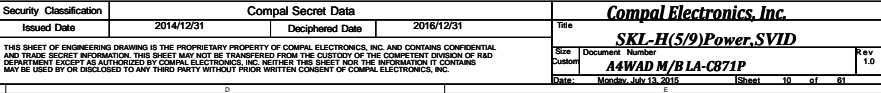
PWR Sequence_SKL-H_DDR3

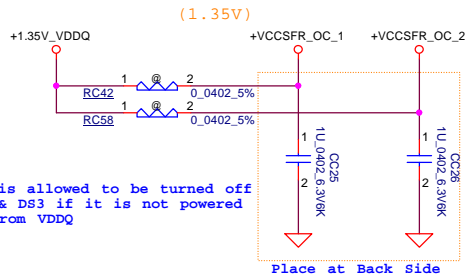
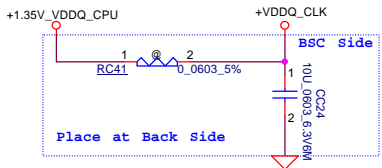
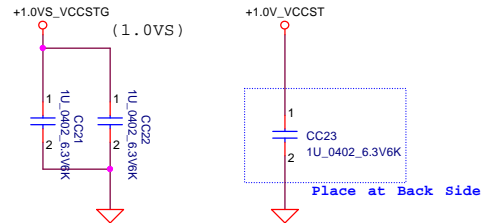
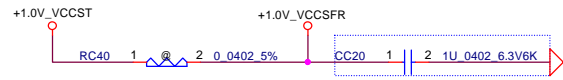


Interleaved Memory

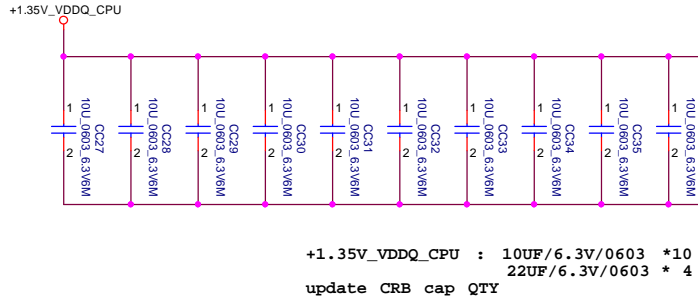


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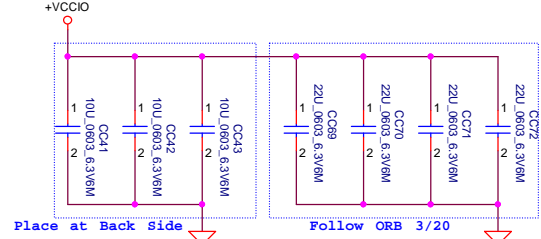
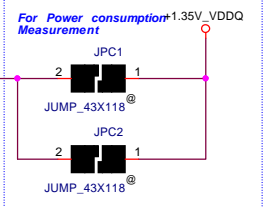
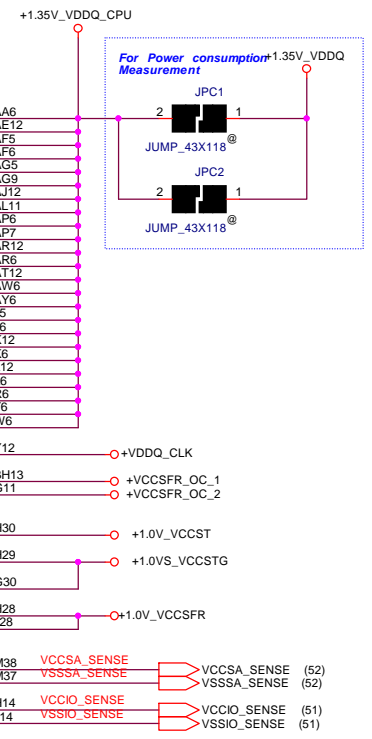
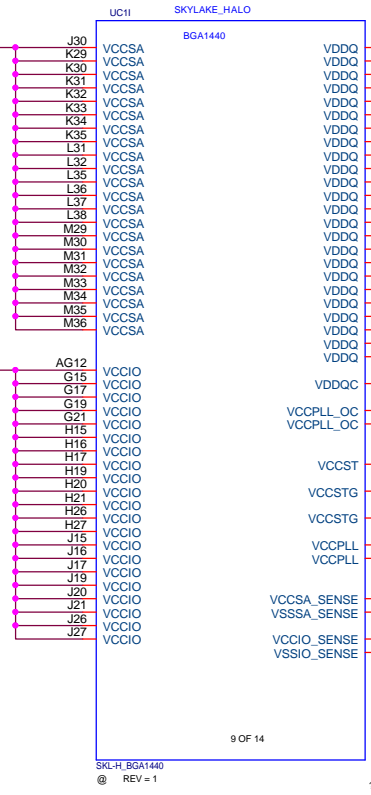
NOTE:
VCCPLL_OC is allowed to be turned off during S3 & DS3 if it is not powered directly from VDDQ



+1.35V_VDDQ_CPU : 10UF/6.3V/0603 *10
22UF/6.3V/0603 * 4
update CRB cap QTY

RVP11 47u*1,10u*7,1u*3
CAP place on PWR side.
+VCCSA

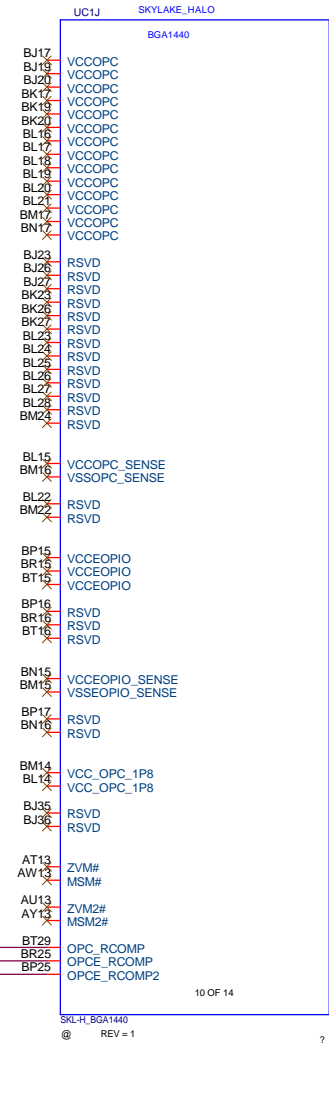
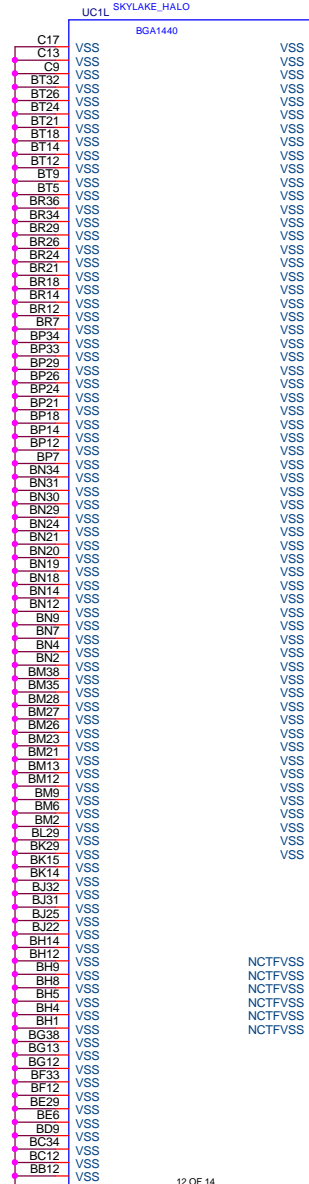
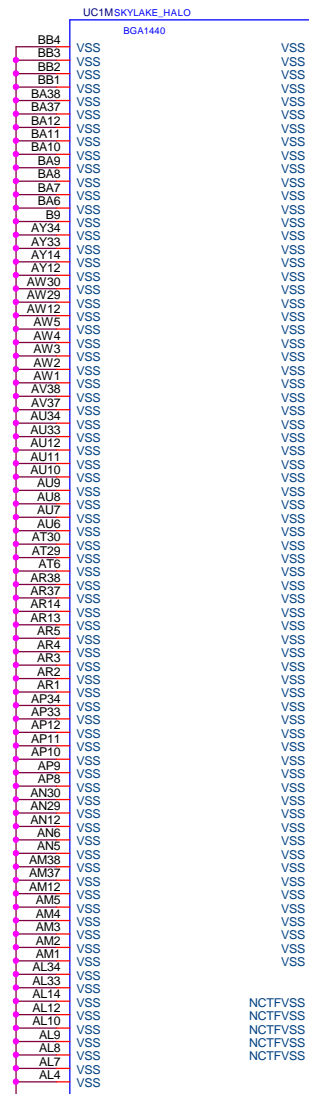
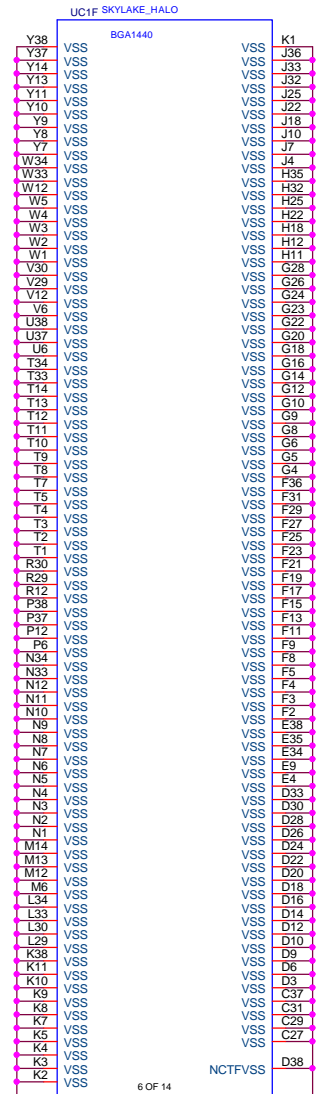
RVP11
PWR NEED PROVIDE +VCCIO
0.95V FOR VCCIO



Follow ORB 3/20

CPU_CORE/VCCGT/VCCSA decoupling capacitor place to PWR side

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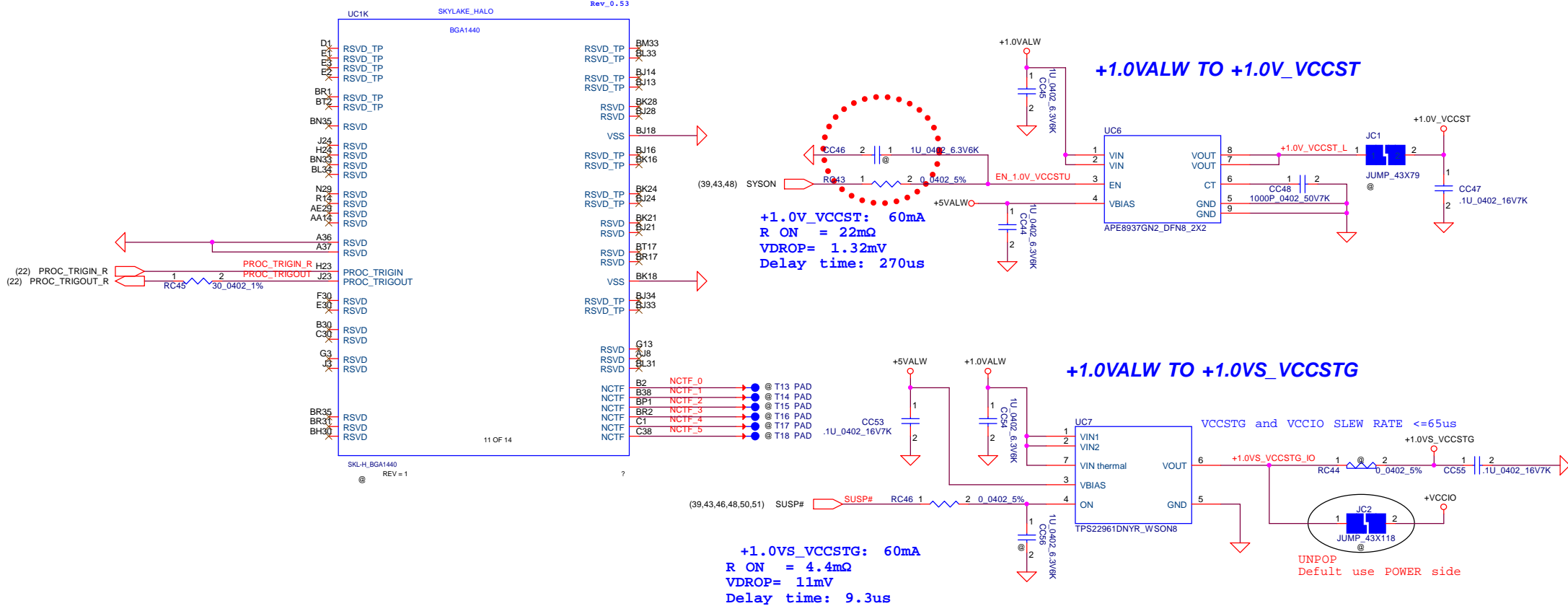


EDRAM

CRB EDRAM

PAD T3824 @ OPC_RCOMP
PAD T3825 @ OPCE_RCOMP
PAD T3826 @ OPCE_RCOMP2

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								Size		Document Number		Rev	
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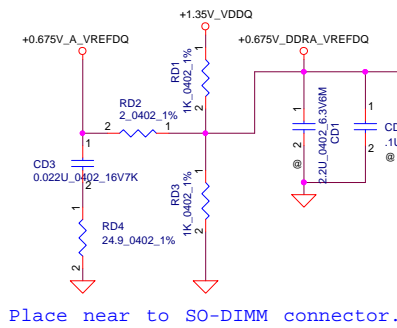
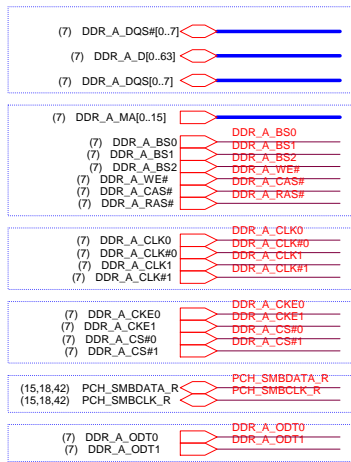


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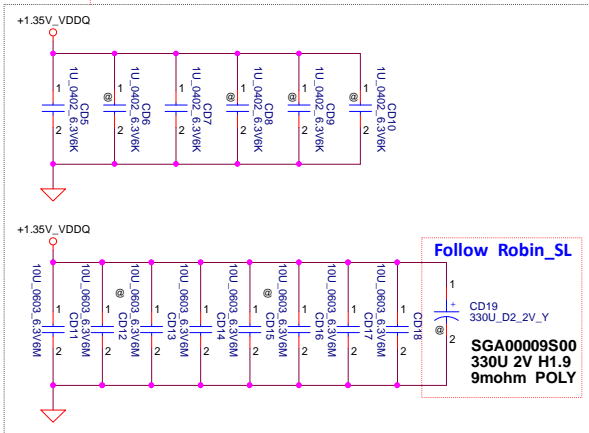
SKL-H(9/9)RSVD

A4WAD M/B LA-C871P



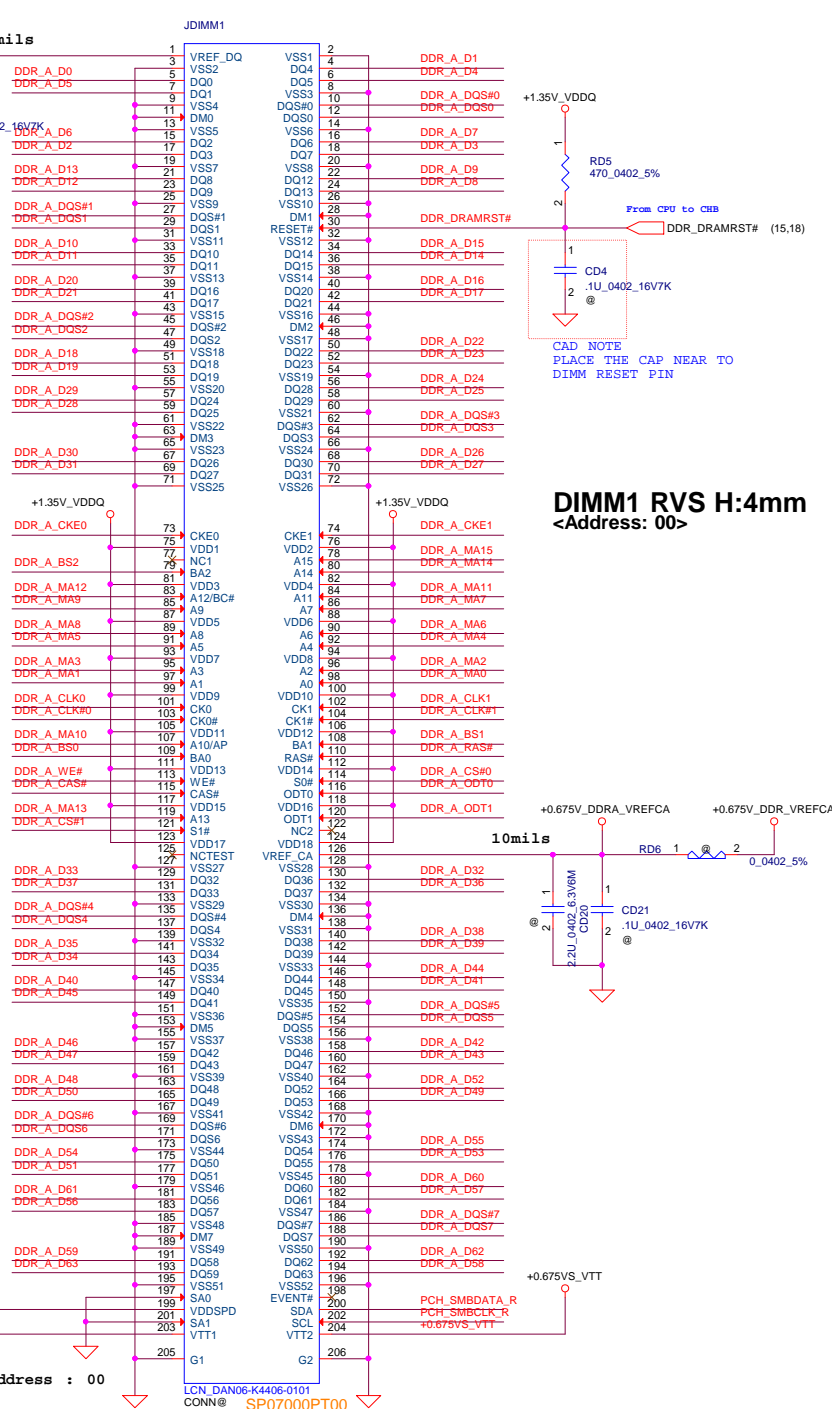
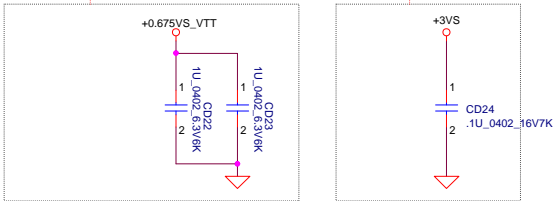
Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket



Layout Note:
Place near JDIMM1.203,204

Layout Note:
Place near JDIMM1.199



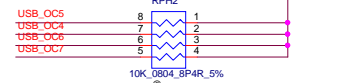
DIMM1 RVS H:4mm
<Address: 00>

Address : 00
LCN_DAN06-K4406-0101
CONN@ SP07000PT00

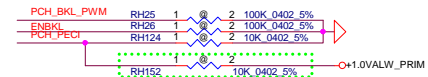
Reverse Type
2-3A to 1 DIMMs/channel

Interleaved Memory

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Functional Strap Definitions

SPI0 MOSI

int. PH

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_MISO

int. PH

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO2

int. PH

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO3

int. PH

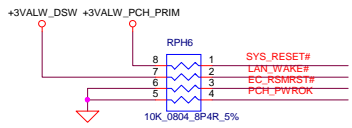
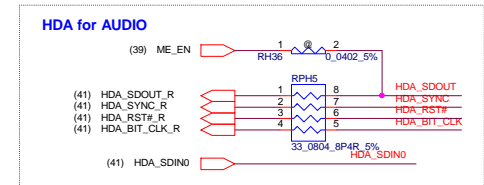
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_H12

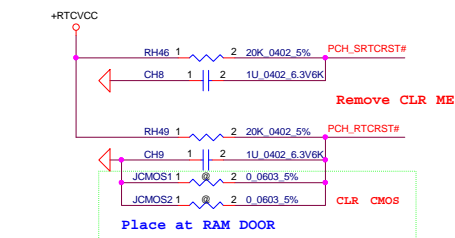
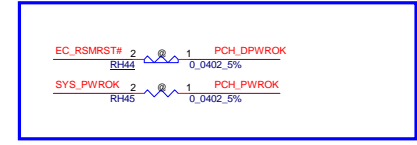
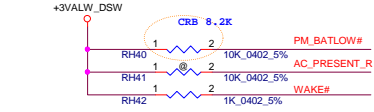
int. PD

This strap should sample LOW.

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Follow 543016_SKL_U_Y_PDG_0_9



Functional Strap Definitions

SMBALERT# / GPP_C2
int. PD
0 = Disable Intel ME (TLS) (Default)
1 = Enable Intel ME (TLS)

SML0ALERT# / GPP_C5
int. PD
0 = LPC is selected for EC. (Default)
1 = eSPI is selected for EC.

SML1ALERT# / PCHHOT# / GPP_B23
int. PD

SPKR / GPP_B14
int. PD
0 = Disable " Top Swap" mod. (Default)
1 = Enable " Top Swap" mod.

HDA_SDO
int. PD
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override).

DDPB_CTRLDATA / GPP_I6
int. PD
0 = Port B is not detected.
1 = Port B is detected. (Default)

DDPC_CTRLDATA / GPP_I8
int. PD
0 = Port C is not detected.
1 = Port C is detected. (Default)

DDPD_CTRLDATA / GPP_I10
int. PD
0 = Port D is not detected. (Default)
1 = Port D is detected.

VGA HDMI

(32) PCH_DP1_HPD

(31) PCH_DP2_HPD

(30) PCH_EDP_HPD

WAKE# (DSX wake event)
10 KΩ pull-up to VccS V0_3
The pull-up is required even if PCIe* interface is not used on the plat f or m

(6) CPU_DISPA_SDO_R
(6) CPU_DISPA_SDI_R
(6) CPU_DISPA_BCLK_R

(41) PCH_DMIC_DATA0
(41) PCH_DMIC_CLK0

(39,43) PCH_PWROK
(6,39) EC_RSMRST#

(SO-DIMM,G-sensor)

(VGA, EC, RTD2168)

(3) PCH_SMBALERT#

(3) PCH_SML0CLK

(3) PCH_SML0DATA

(3) PCH_SML1CLK

(3) PCH_SML1DATA

(3) PCH_SML2CLK

(3) PCH_SML2DATA

(3) PCH_SML3CLK

(3) PCH_SML3DATA

(3) PCH_SML4CLK

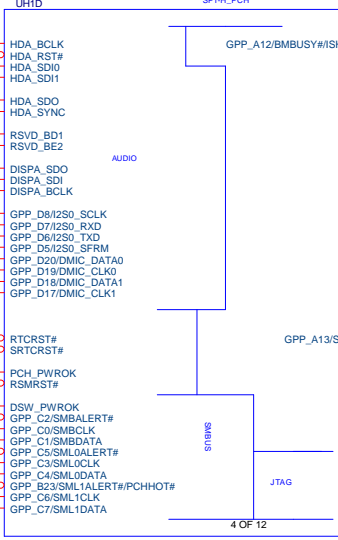
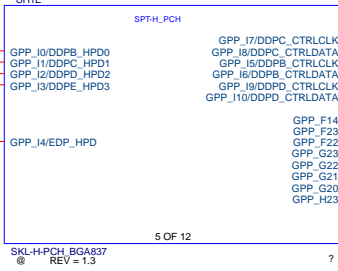
(3) PCH_SML4DATA

(3) PCH_SML5CLK

(3) PCH_SML5DATA

(3) PCH_SML6CLK

(3) PCH_SML6DATA



(3) PCH_SMBALERT#

(3) PCH_SML0CLK

(3) PCH_SML0DATA

(3) PCH_SML1CLK

(3) PCH_SML1DATA

(3) PCH_SML2CLK

(3) PCH_SML2DATA

(3) PCH_SML3CLK

(3) PCH_SML3DATA

(3) PCH_SML4CLK

(3) PCH_SML4DATA

(3) PCH_SML5CLK

(3) PCH_SML5DATA

(3) PCH_SML6CLK

(3) PCH_SML6DATA

PCH_DP2_CTRL_CLK

PCH_DP2_CTRL_DATA

PCH_DP1_CTRL_CLK

PCH_DP1_CTRL_DATA

PCH_DP2_CTRL_CLK

PCH_DP2_CTRL_DATA

PCH_DP1_CTRL_CLK

PCH_DP1_CTRL_DATA

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PCH_DP2_CTRL_CLK

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PCH_DP2_CTRL_DATA

PCH_DP1_CTRL_CLK

PCH_DP1_CTRL_DATA

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PCH_DP1_CTRL_CLK

PCH_DP1_CTRL_DATA

PCH_DP2_CTRL_CLK

PCH_DP2_CTRL_DATA

PCH_DP1_CTRL_CLK

PCH_DP1_CTRL_DATA

PCH_DP2_CTRL_CLK

PCH_DP2_CTRL_DATA

PCH_DP1_CTRL_CLK

PCH_DP1_CTRL_DATA

PCH_DP2_CTRL_CLK

PCH_DP2_CTRL_DATA

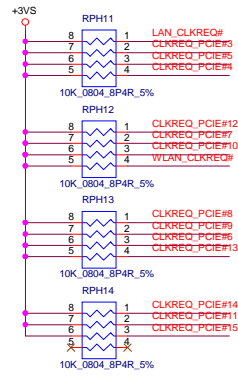
PCH_DP1_CTRL_CLK

PCH_DP1_CTRL_DATA

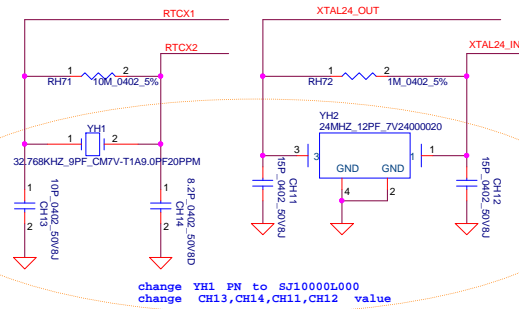
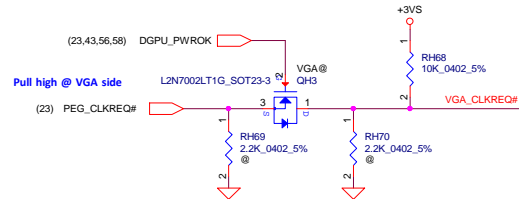
PCH_DP2_CTRL_CLK

PCH_DP2_CTRL_DATA

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Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	PCH(3/7)GPIO,SMBUS
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				Sheet	18 of 61



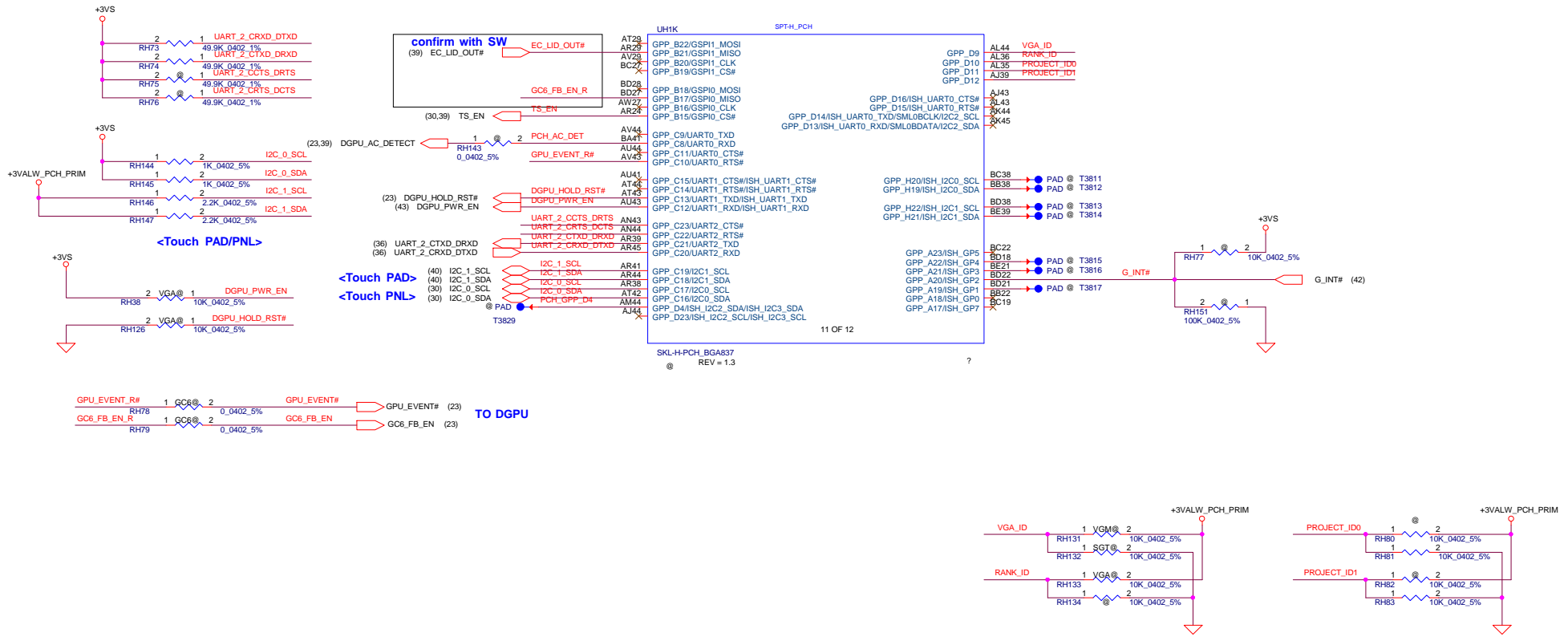
Follow PDG 0.71 Table 52-17
10/13 Dan
CHECK NEEDED IF UNUS#?



Functional Strap Definitions

GSP11_MOSI / GPP_B22
int. PD
Boot BIOS Destination
0 = SPI (Default)
1 = LPC

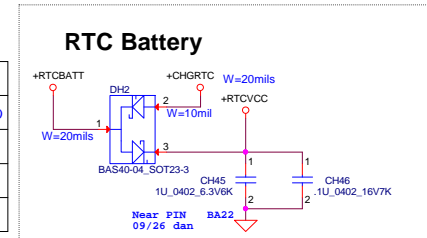
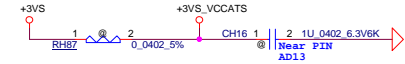
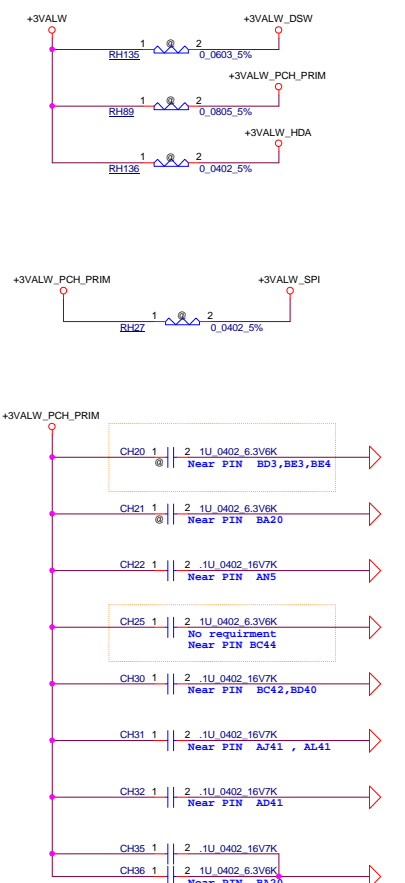
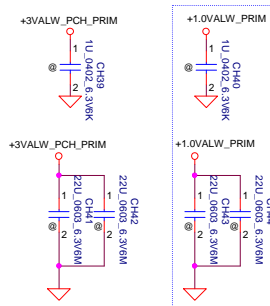
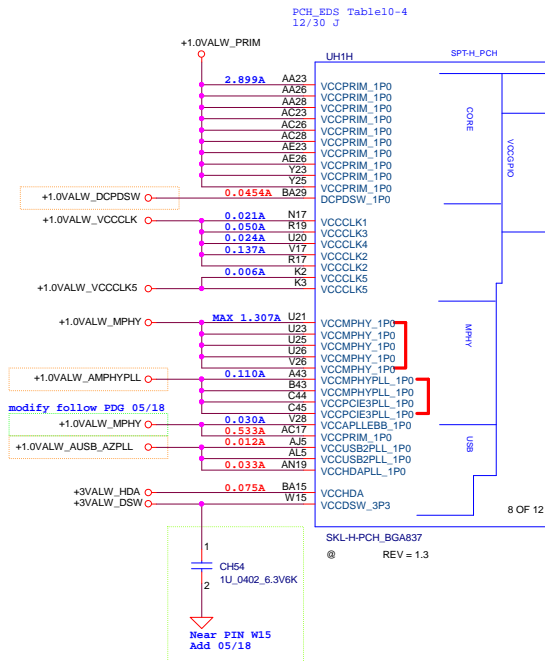
GSP10_MOSI / GPP_B18
int. PD
0 = Disable " No Reboot " mode (Default)
1 = Enable " No Reboot " mode (PCH will disable the TCO
Timer system reboot feature).



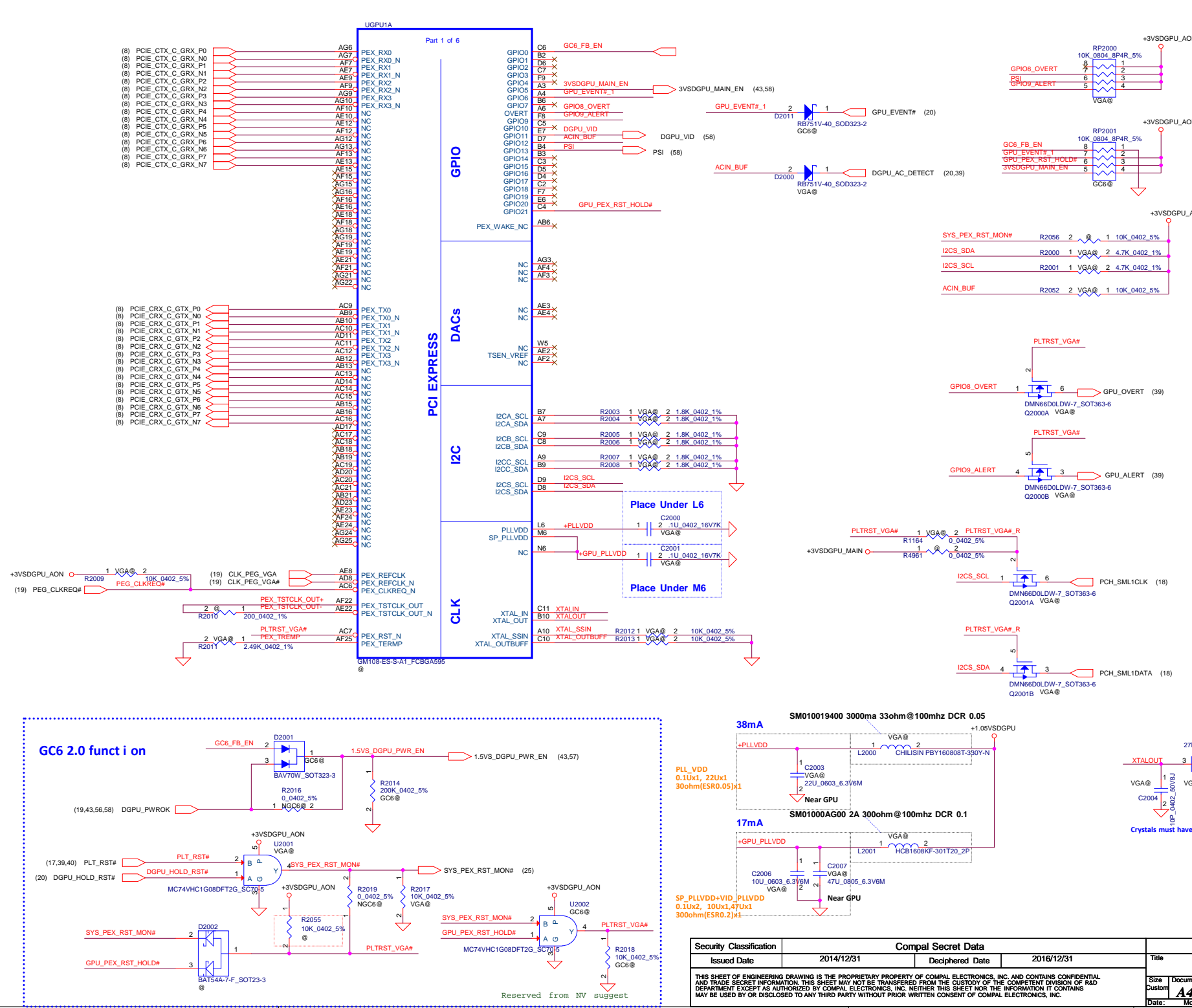
VGA_ID	GPP_D9
SGT	0
VGM	1

RANK_ID	GPP_D10
DR	0
SR	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
* A4WAD	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1



Security Classification		Compal Secret Data		Compal Electronics, Inc. PCH(6/7)POWER	
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				Custom	
				A4WAD M/B LA-C871P Date: Monday, July 13, 2015 Sheet 21 of 61	
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GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		



```

ROM_SI pull down 15kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x2
ROM_SI pull down 10kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x3
ROM_SI pull down 25kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x1
ROM_SI pull up 35kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x0
ROM_SI pull up 30kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0xD
ROM_SI pull down 30kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x0
ROM_SI pull up 25kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0xC

```

N16SGT Option Component

```
ROM_SI pull down 4.99kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x0
ROM_SI pull down 10kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x1
ROM_SI pull down 15kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x2
ROM_SI pull down 20kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x3
ROM_SI pull down 25kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x4
ROM_SI pull down 30kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x5
```

Decive ID : 0x1347

Decive ID : 0x1299

Diagram illustrating the relationship between two DNA sequences, X7607 and X7608, and their associated markers.

Sequence X7607 is associated with GM2G SAM-N 256M16G and X76614BOL57.

Sequence X7608 is associated with X76614BOL58 and GM2G SAM-N 256M16G.

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Date: Monday, July 13, 2015				Sheet 25	of 61

GPU Package Type	Capacitor Type	Footprint	Population	Location	
GB2B-64 DDR3	0.1 μ F X7R	0402	2	2	Under GPU
	1 μ F X7R	0603	2	2	Under GPU
	4.7 μ F X6S	0603	2	2	Under GPU
	10 μ F X5R	0805	1	1	Near GPU
	22 μ F X5R	0805	1	1	Near GPU

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64	1.0 μ F X6S	0402	1	Under GPU
	4.7 μ F X6S	0603	1	Near GPU
	10 μ F X5R	0805	1	Midway between GPU and Power Supply
	22 μ F X5R	0805	1	Midway between GPU and Power Supply

GPU Package

GPU Package	Rail
GB2B-64	3V3_MAIN
GB4B-128	
GB3-256	
GB2B-64	3V3_AON
GB4B-128	
GB3-256	

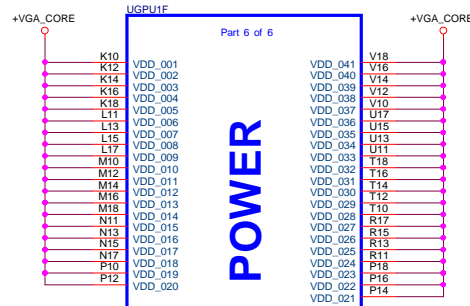
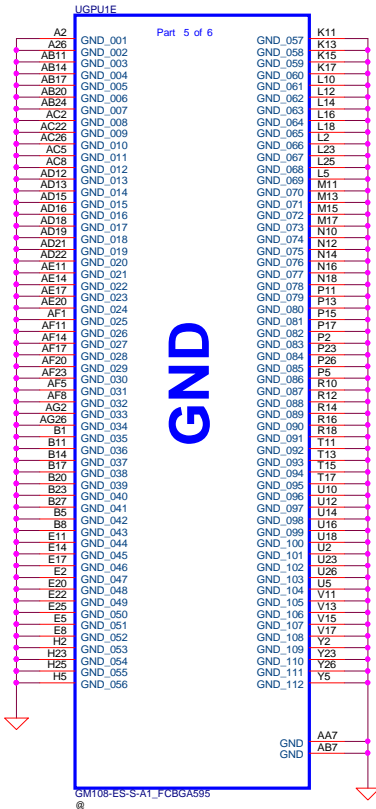
Capacitor Type

Capacitor Type	Value	Part
0.1 μ F	X5R	
4.7 μ F	X5R	
0.1 μ F	X6S	
1.0 μ F	X6S	
4.7 μ F	X5R	

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AOH	0.1µF	X6S	0402	1	1	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μ F	X5R	0402	1	Near GPU
4.7 μ F	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μ F	X6S	0402	1	Under GPU
1.0 μ F	X5R	0603	1	Near GPU
4.7 μ F	X5R	0805	1	Near GPU



NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint	Population	Location	Comments
GB2B-64	4.7 μ F	X6S	0603	10	10	Under GPU
	1 μ F	X6S	0402	4	4	Under GPU
	47 μ F	X5R	0805	1	1	Near GPU
	22 μ F	X5R	0805	1	1	Near GPU
	4.7 μ F	X5R	0805	5	5	Near GPU
	330 μ F	POS	7343	1	1	Near GPU ESR \leq 6 m Ω

DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core	FB Total	1.05V Total
		—	1.5/1.35V	1.05V
N155-GM	DDR3/L	48.11	4.23	0.91
N155-GT	DDR3/L	60.07	4.26	0.91

DA-06925-V05

Table 6. EDP-Peak at $T_J = 102^\circ\text{C}$

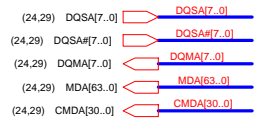
Power Supply Rail (V)	N15V-GM-S DDR3/L
	(A)
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

DA07075-V01

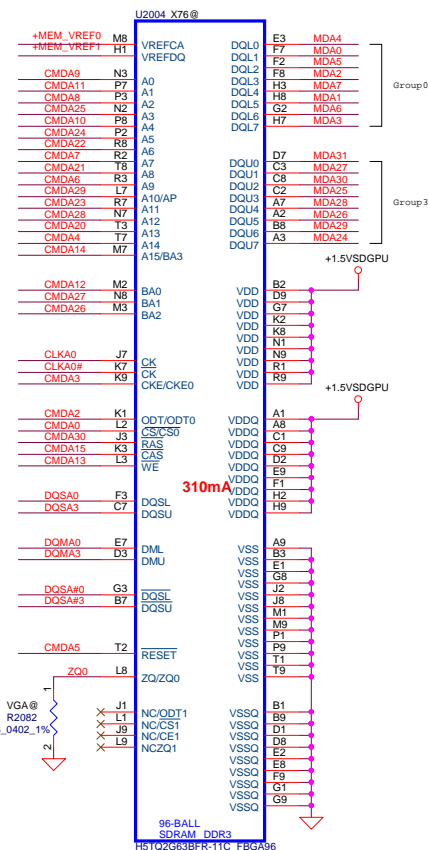
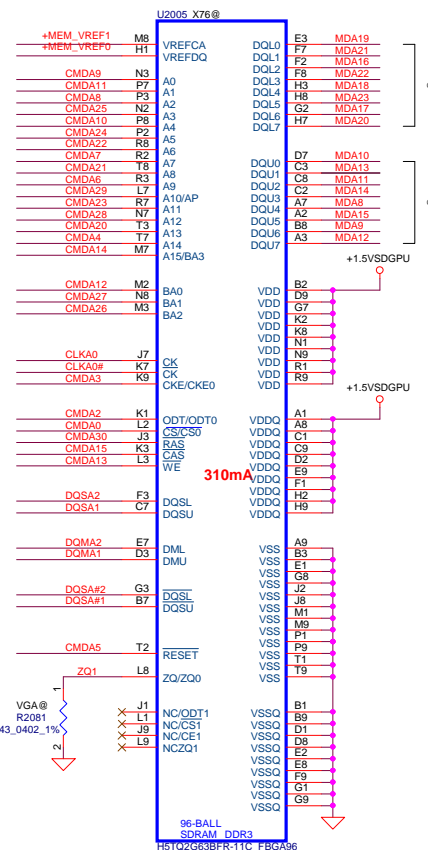
Table 7. EDP-Peak at $T_J = 102^\circ\text{C}$

Power Supply Rail (V)	N15V-GL DDR3
	(A)
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

VRAM DDR3 chips



LOW BIT



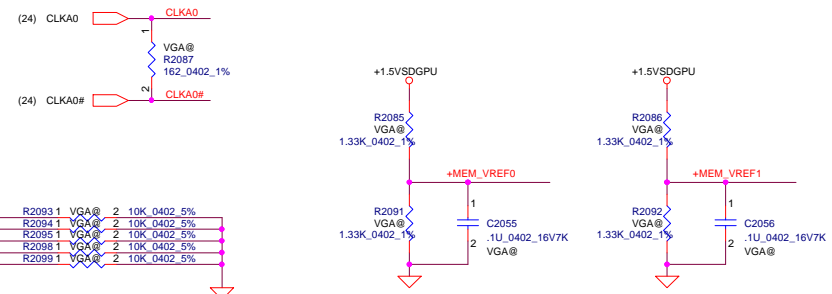
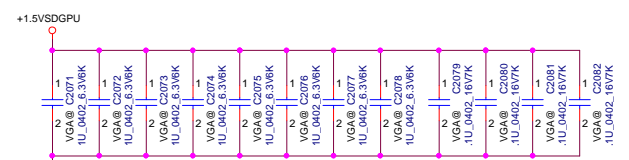
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

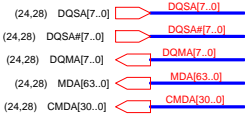
Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CAS*	No Termination

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

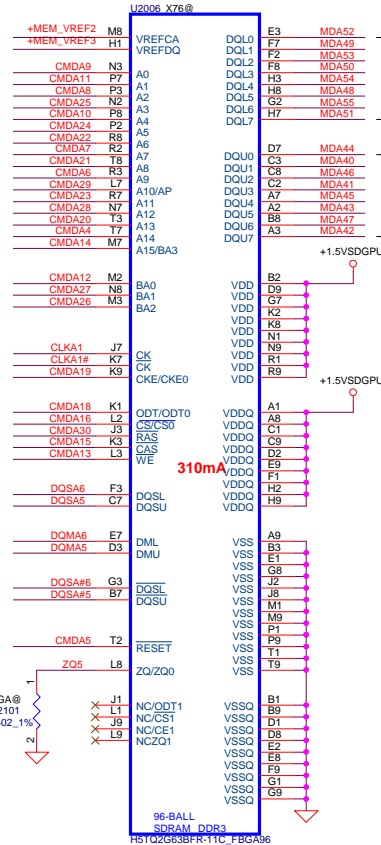
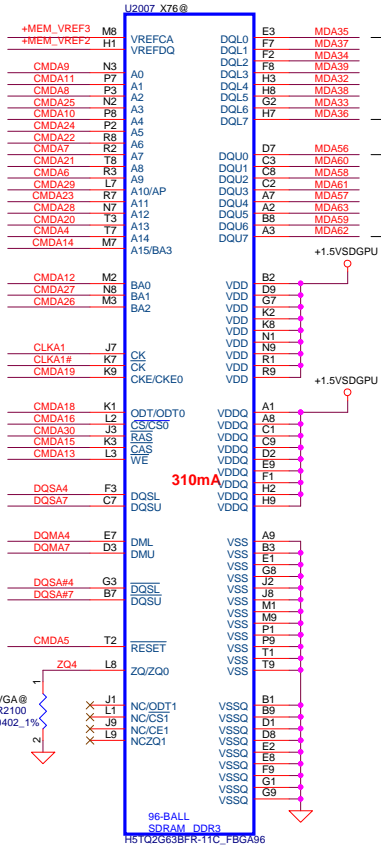
Capacitor Type		Population		Location
FBVDD/Q Combined		FBVDDQ	FBVDD	
0.1 μF	X7R	0402	2	Under DRAM
1.0 μF	X7R	0603	4	Under DRAM
10 μF	X5R	0805	0	Close to DRAM



VRAM DDR3 chips



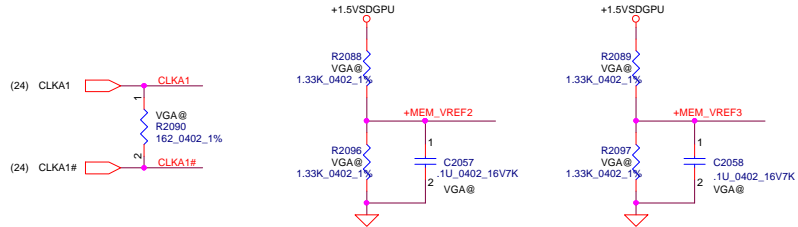
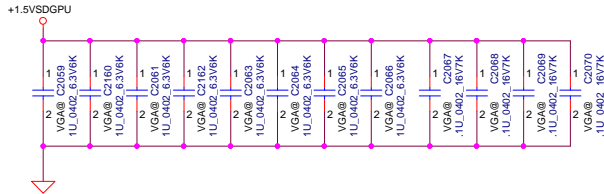
HIGH BIT



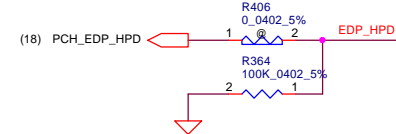
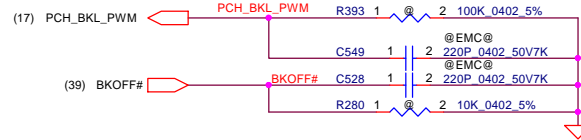
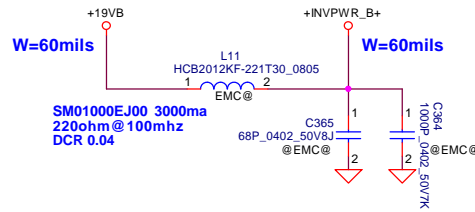
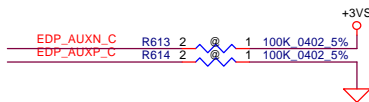
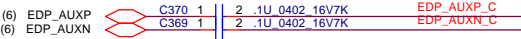
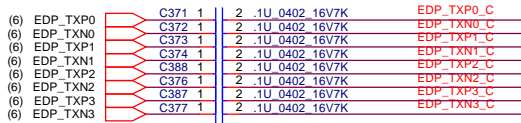
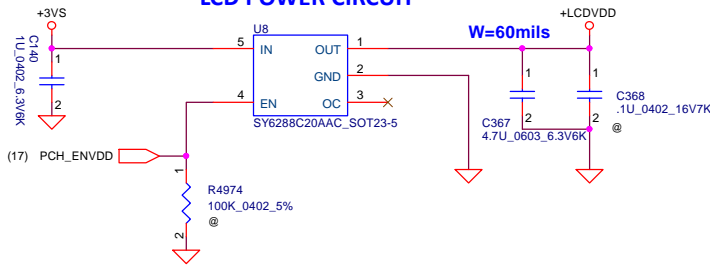
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

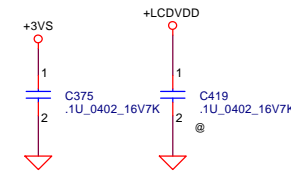
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



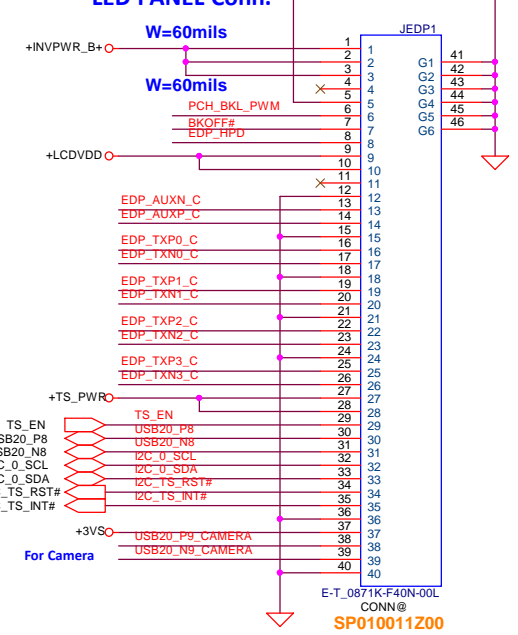
LCD POWER CIRCUIT



Place closed to JEDP1

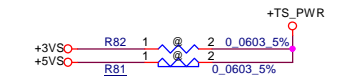


LED PANEL Conn.



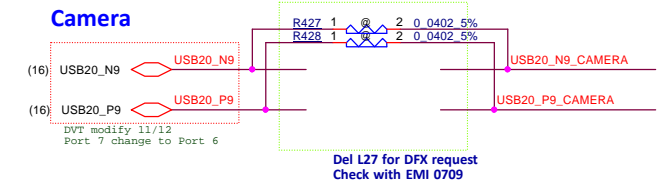
Touch Screen

I2C Touch Screen

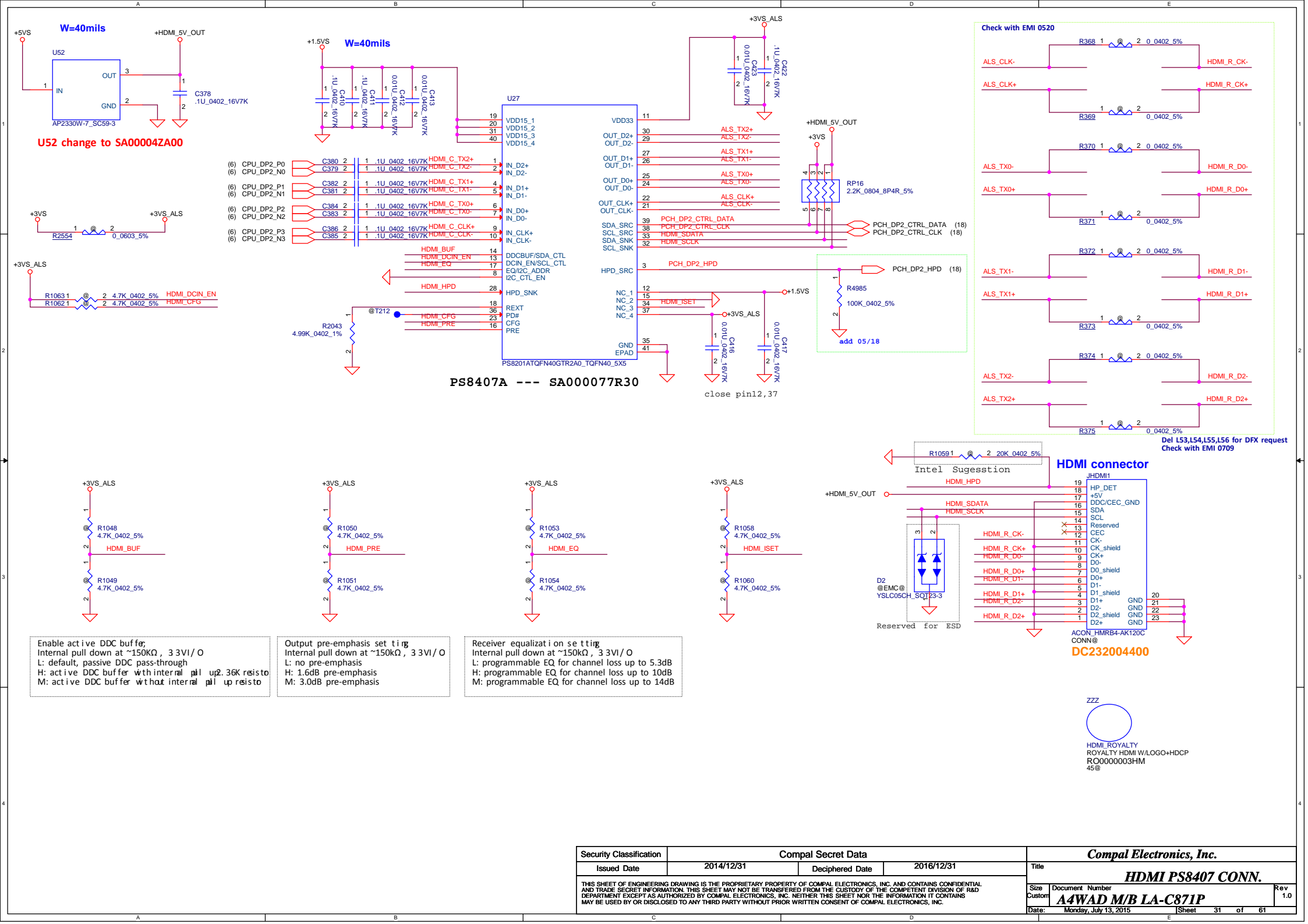


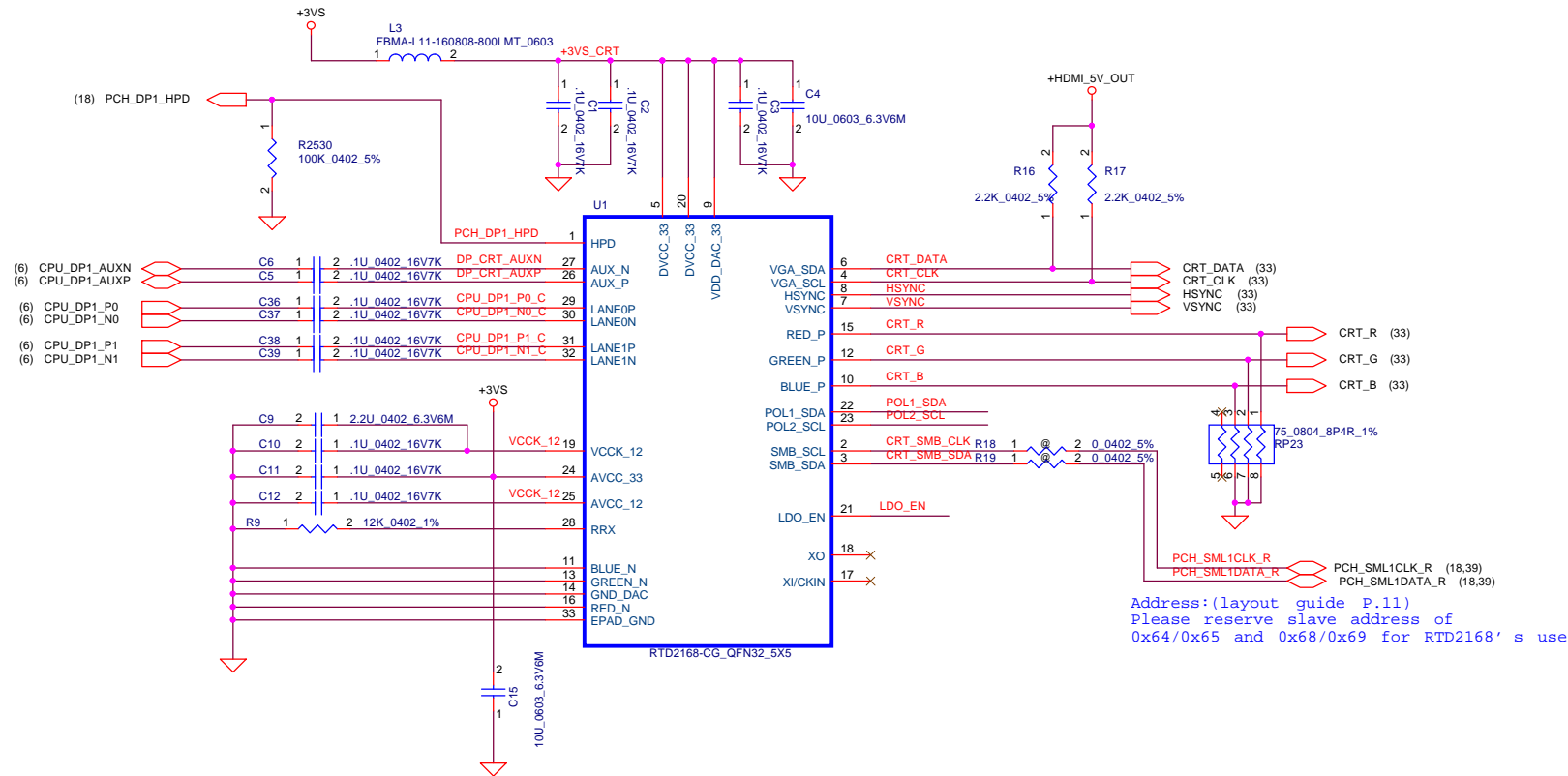
SPI touch RST follow CRB #544669 P.8

Camera



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						Size Custom		Document Number		Rev 1.0	
						Date: Monday, July 13, 2015		Sheet 30 of 61		A4WAD M/B LA-C871P	

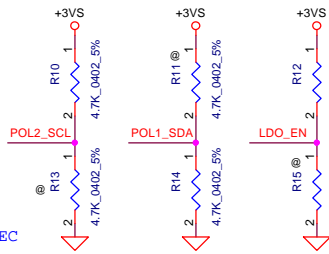




Address:(layout guide P.11)
Please reserve slave address of
0x64/0x65 and 0x68/0x69 for RTD2168' s use

		POL_SDA	
POL_SCL	0	X	EP
	1	*ROM	EEPROM

ROM: Internal ROM
EP: Programmed external EC
EEPROM: External ROM

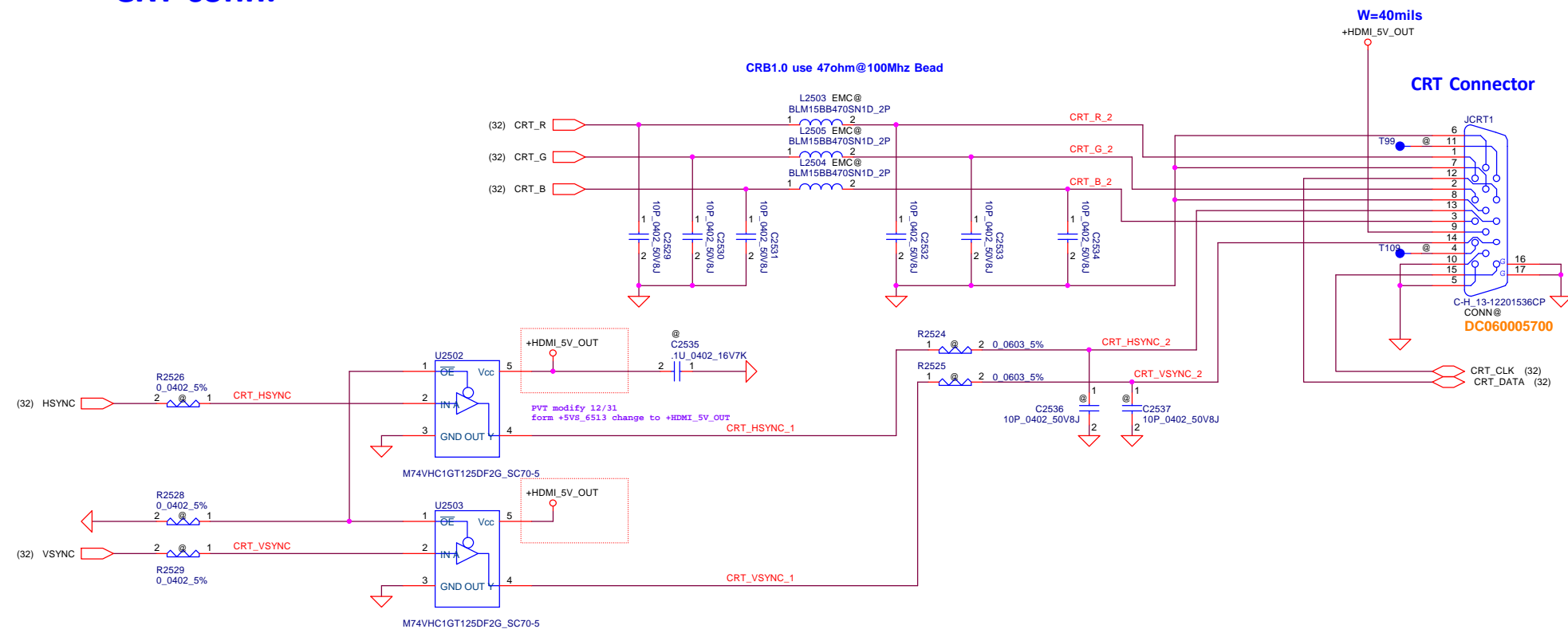


LDO_EN:
*1: Internal 1.2V
0: External 1.2V

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				CRT Realtek RTD2168	
				Size	Rev
				Custom	1.0
				Document Number	
				A4WAD M/B LA-C871P	
				Date: Monday, July 13, 2015	Sheet 32 of 61

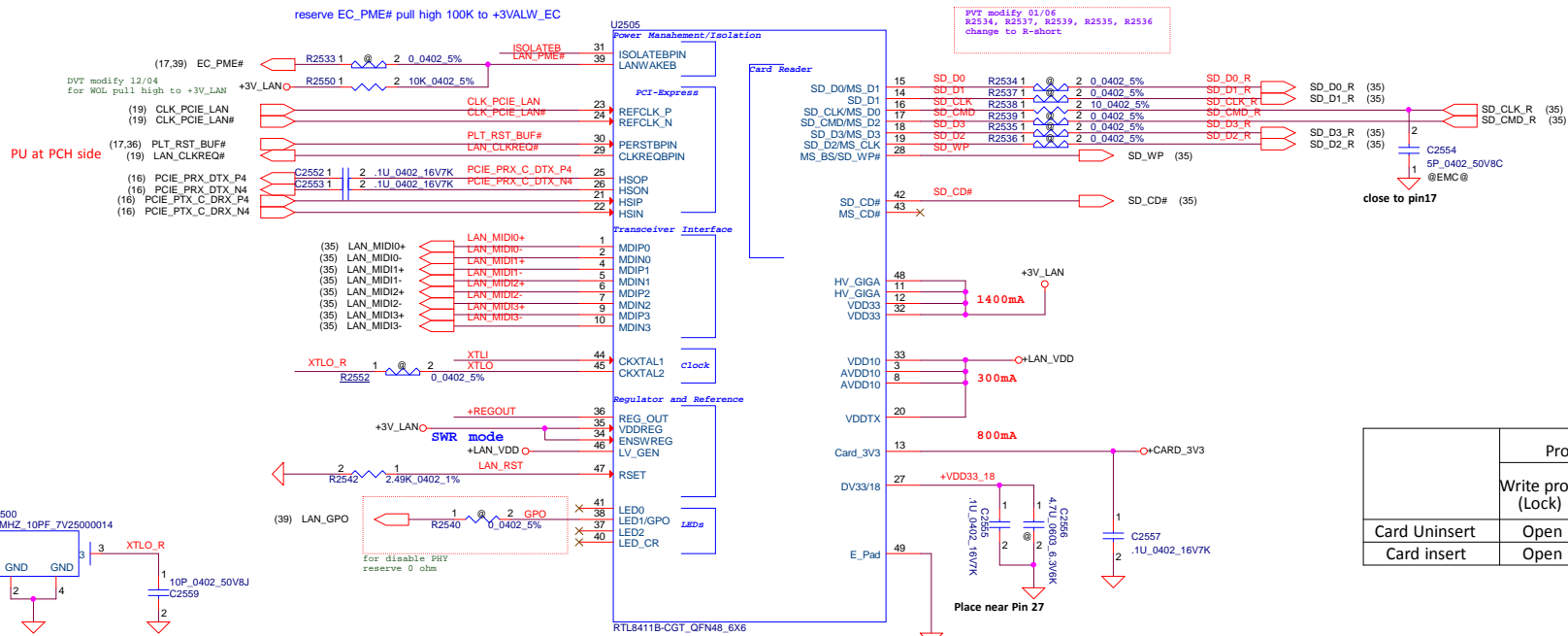
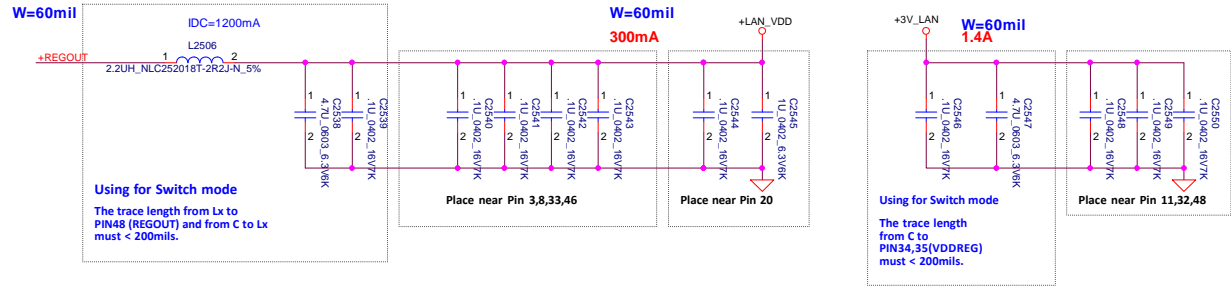
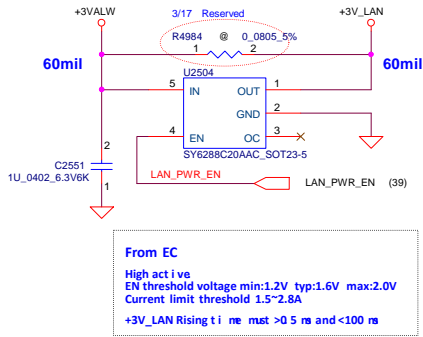
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CRT conn.

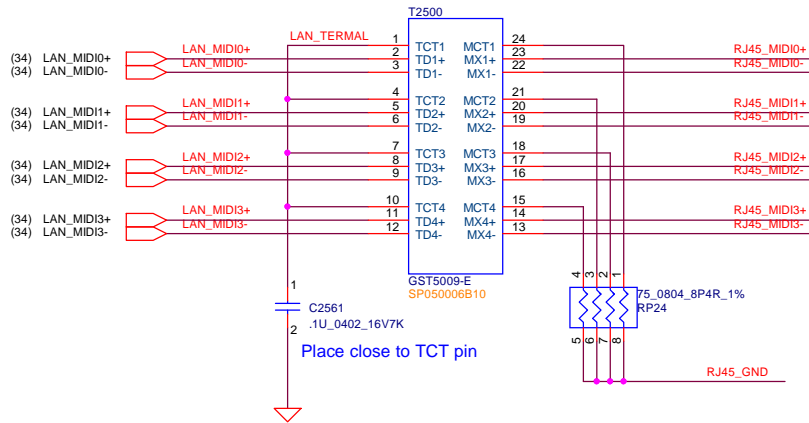


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								Size	Document Number	Rev
								Custom	A4WAD M/B LA-C871P	1.0
								Date:	Monday, July 13, 2015	Sheet

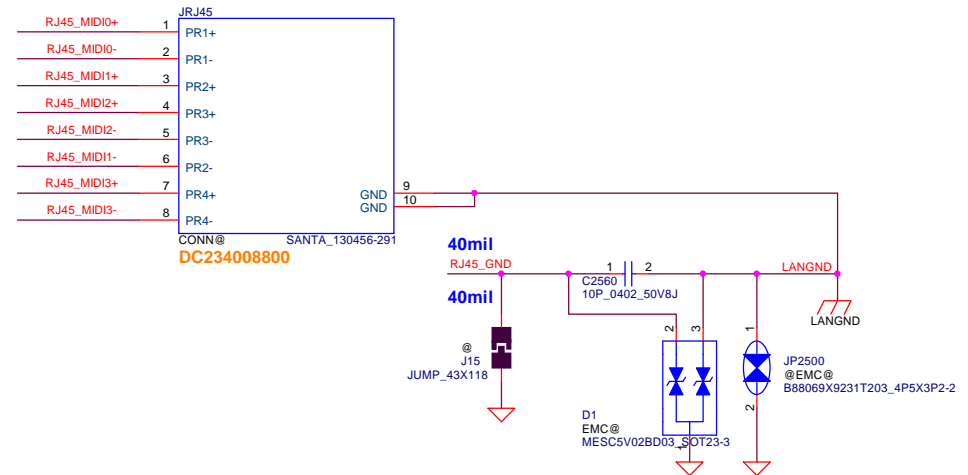
LAN-RTL8411B



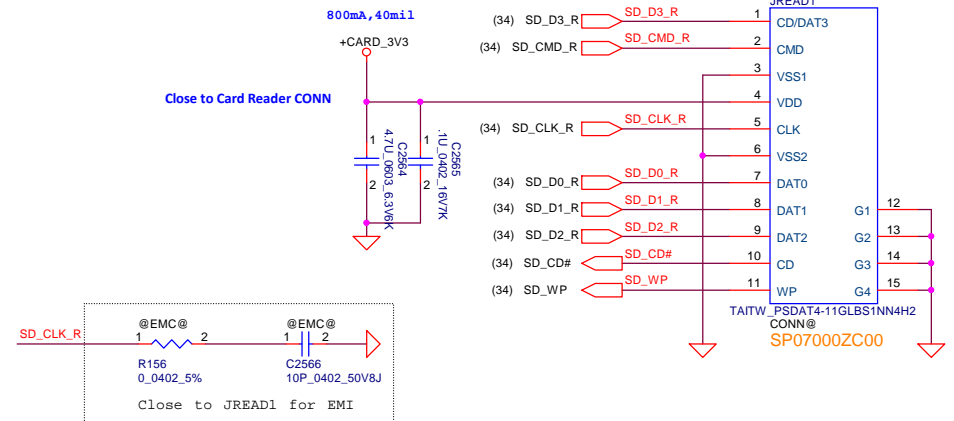
	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close



LAN Connector

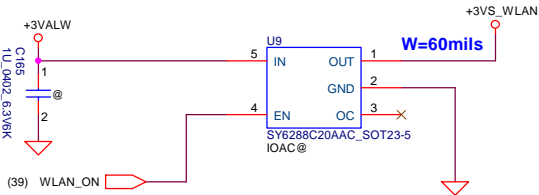
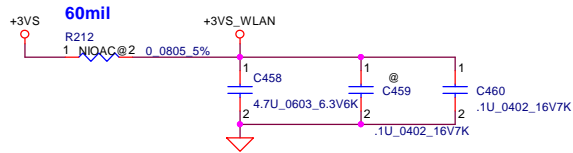


Card Reader Connector



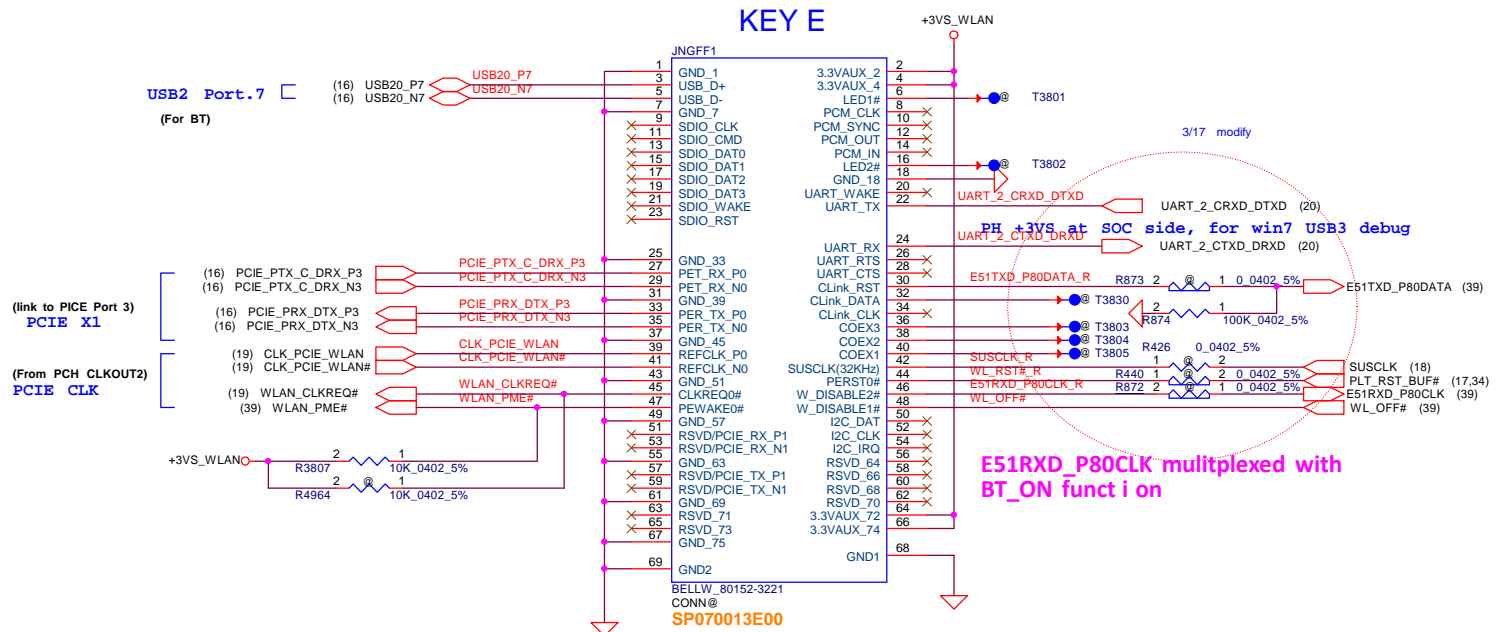
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						Size		Document Number		Rev	
						Custom		A4WAD M/B LA-C871P		1.0	
						Date:		Monday, July 13, 2015		Sheet 35 of 61	

Wireless LAN



NGFF WL+BT (KEY E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UM_Power_SPC/GPIO/PEWake1#	RESERVED/REFCLKP1	71
68	UM_Power_SNK/CLKREQ1#	GND	69
66	UM_SWP/PERST1#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (IO/3.3)	GND	63
60	DC CLK (IO/3.3)	Reserved/PERn1	61
58	DC DATA (IO/3.3)	Reserved/PERp1	59
56	W_DISABLE# (IO/3.3V)	GND	57
54	Reserved/W_DISABLE# (IO/3.3V)	RESERVED/REFCLKN1	55
52	PERST0# (IO/3.3V)	RESERVED/REFCLKP1	53
50	SUSCLK(32KHz) (IO/3.3V)	CLKREQ0# (IO/3.3V)	51
48	CODEX1 (IO/0.1.8V)	GND	49
46	CODEX2 (IO/0.1.8V)	REFCLKP0	47
44	CODEX3 (IO/0.1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (IO/0.1.8V)	PERn0	37
34	UART CTS (IO/0.1.8V)	PERp0	35
32	UART Tx (IO/0.1.8V)	GND	33
30	UART Rx (IO/0.1.8V)	SDIO_RESET# (IO/0.1.8V)	29
28	UART Wake# (IO/3.3V)	SDIO_WAKE# (IO/0.1.8V)	27
26	GND	SDIO_DAT3 (IO/0.1.8V)	25
24	LED#1 (V/CO)	SDIO_DAT2 (IO/0.1.8V)	23
22	PCM_OUT/IO/SD_OUT (IO/0.1.8V)	SDIO_DAT1 (IO/0.1.8V)	21
20	PCM_IN/IO/SD_IN (IO/0.1.8V)	SDIO_CMD (IO/0.1.8V)	19
18	PCM_SYNC/IO/SD_IN (IO/0.1.8V)	SDIO_CLK (IO/0.1.8V)	17
16	PCM_CLK/IO/SD_IN (IO/0.1.8V)	GND	15
14	LED#1 (V/CO)	GND	13
12	3.3V	USB_D-	11
10	3.3V	USB_D+	9
8	GND	GND	7
6	GND	GND	5
4	GND	GND	3
2	GND	GND	1



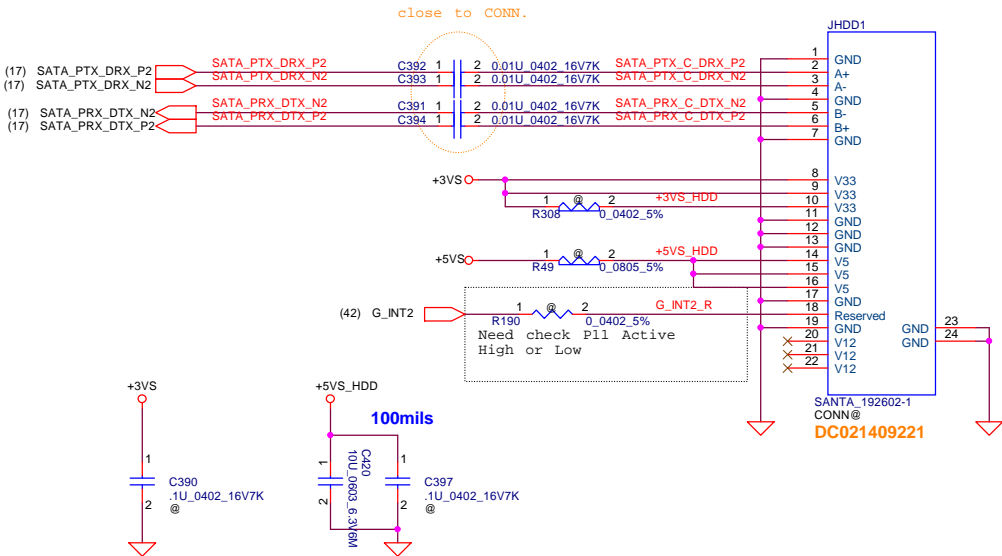
3.4-8.4-3.1.7.1. UART Wakeup

The UART power management protocol supports the following 4-wire and 5-wire interfaces:

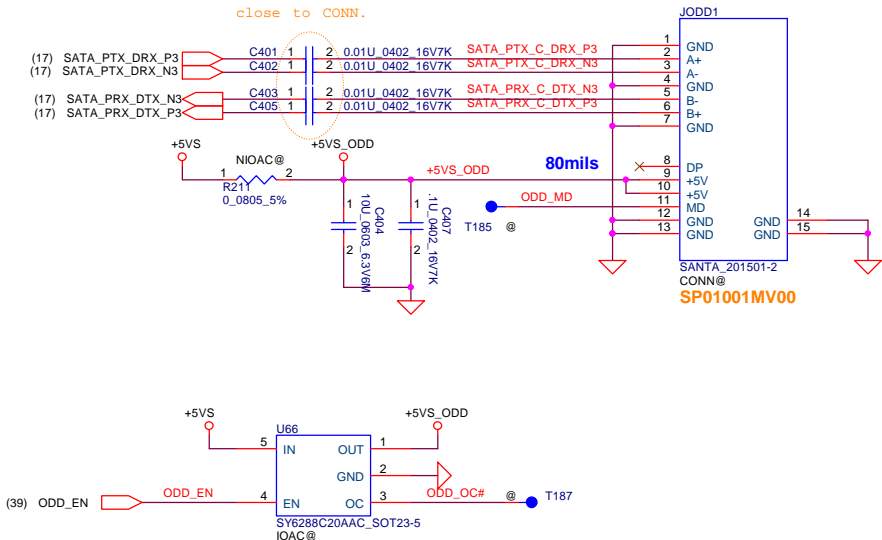
- ☐ ~~RDX~~ **UART_RXD** (Input): Receive Data
- ☐ ~~RTX~~ **UART_TXD** (Output): Transmit Data
- ☐ **UART_RTS** (Input): Request to Send (Host Flow Control)
- ☐ **UART_CTS** (Output): Clear to Send (Device Flow Control)
- ☐ ~~Host Wake Up~~ **UART_Wake#** (Output): Host wake-up line is optional in case the host support in band wake-up

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				Size	Document Number	Rev
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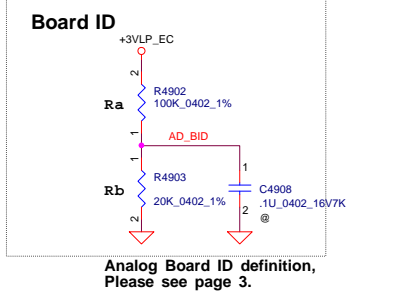
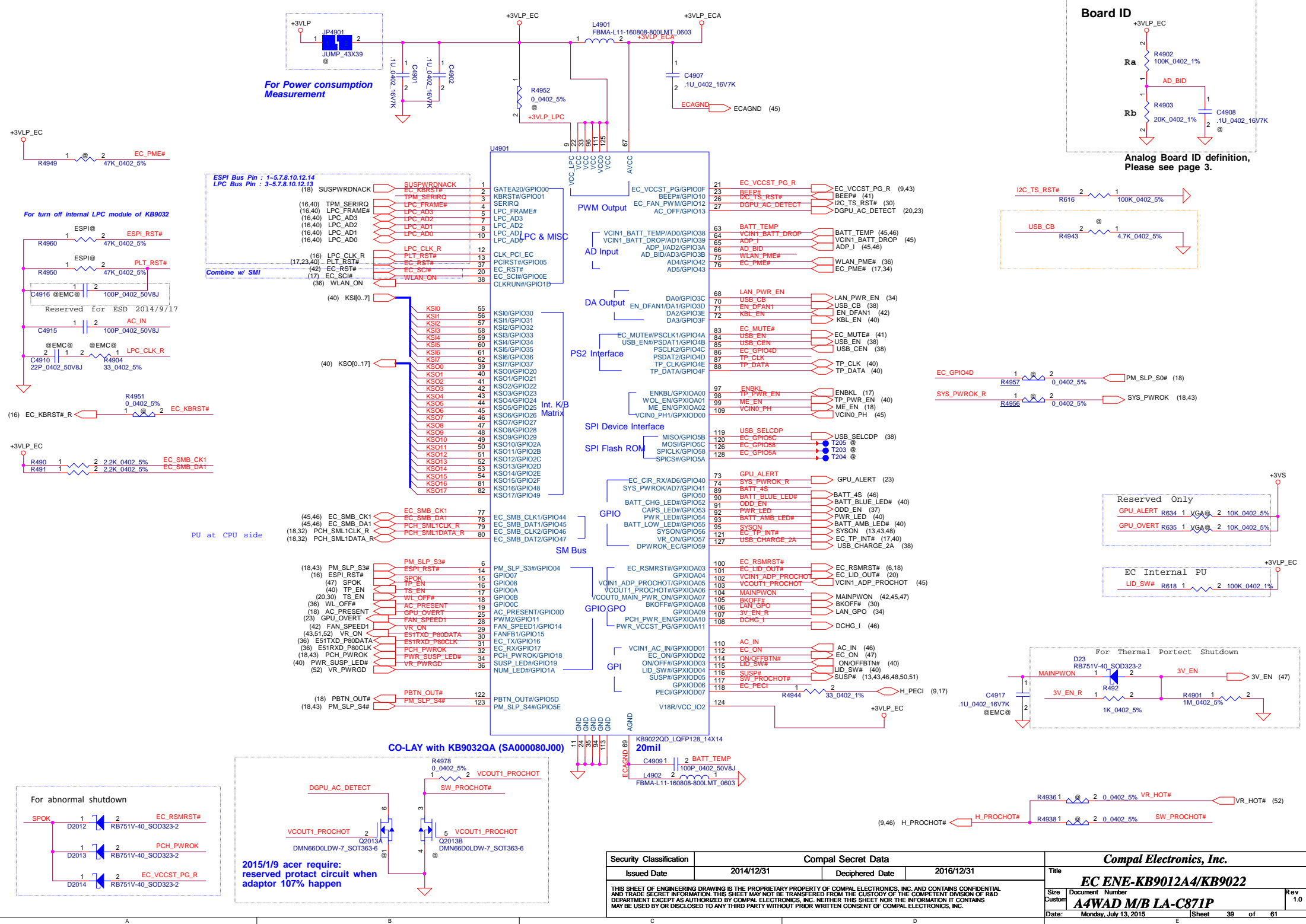
SATA HDD Conn.



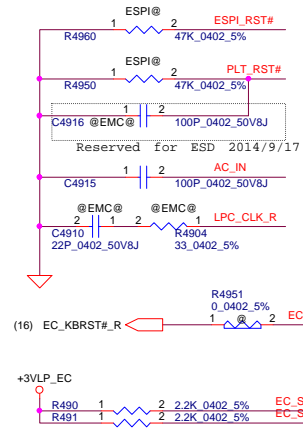
SATA ODD Conn.



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		Size Custom		Document Number				Rev 1.0	
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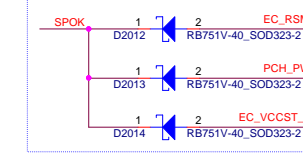
For turn off internal LPC module of KB9032



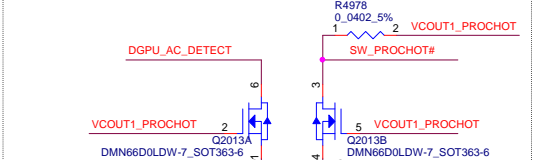
PU at CPU side



For abnormal shutdown

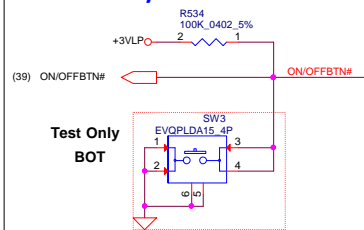


2015/1/9 acer require:
reserved protect circuit when
adaptor 107% happen

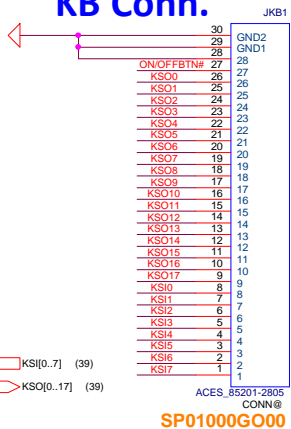


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ON/OFF BTN

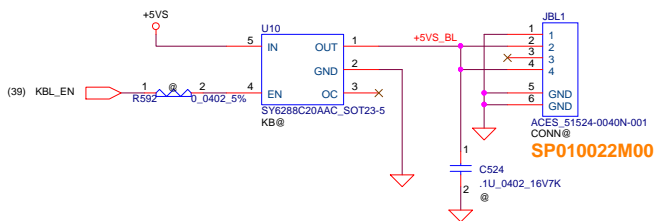


KB Conn.



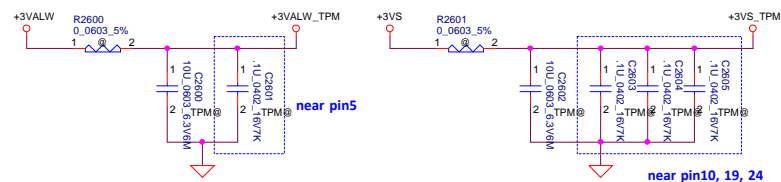
SP01000G000

KB BackLight Conn. Reserve



SP010022M00

TPM Board for 2015



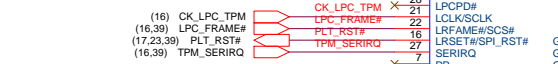
BADD	SELECTION
0	EEh - EFh
1	7Eh - 7Fh

GPIO3/BADD with Internal PH (default)

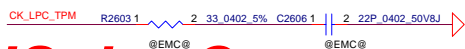
CLKRUN PH 10K to +3VS at PCH side



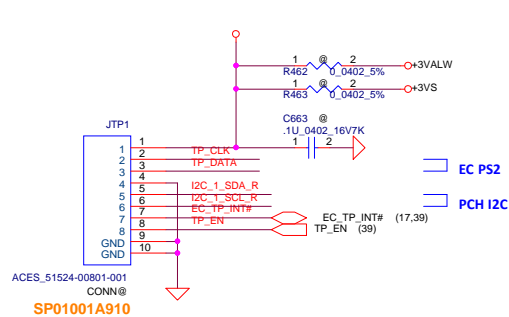
LPCPD# had internal PH



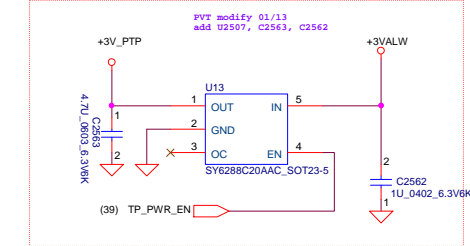
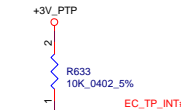
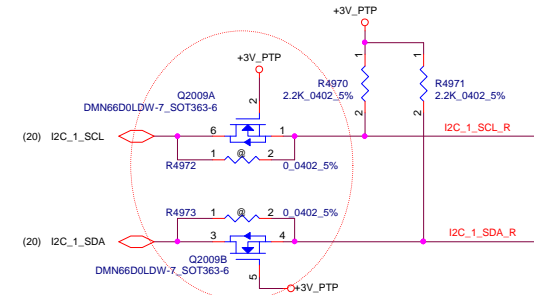
SERIRQ PH 10K to +3VS at PCH side



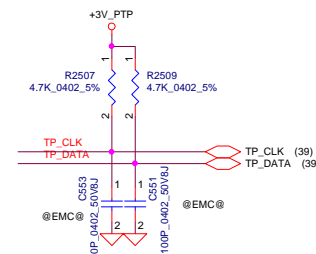
TP/B Conn.



SP01001A910

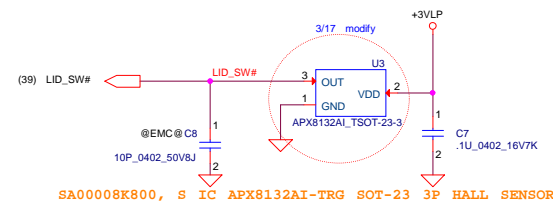


TP_PWR_EN follow SYSON behavior



Lid Switch

(Hall Effect Switch)



SA00008K800, S IC APX8132AI-TRG SOT-23 3P HALL SENSOR

Dual Amber+Blue

LTST-S115TBKF-CA (SC50000C500)

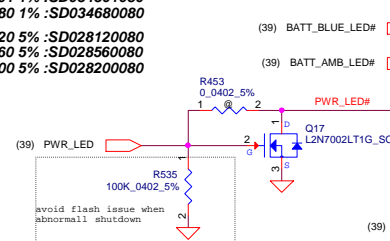
Vf @ 5 mA :

UD5: 1.7 ~ 2.3V
(3.3-1.7)/300=5.71 mA
(3.3-2.3)/300=3.57 mA
R min: 100 ohm
R max: 700 ohm

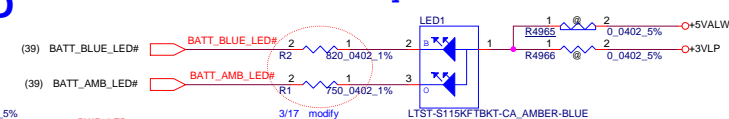
CB5: 2.65-3.05V
(3.3-2.65)/50=13.00 mA
(3.3-3.05)/100=5.0 mA
R min: 50 ohm
R max: 475 ohm

100 1% :SD034100080
150 1% :SD034150080
301 1% :SD034301080
680 1% :SD034680080
120 5% :SD028120080
560 5% :SD028560080
200 5% :SD028200080

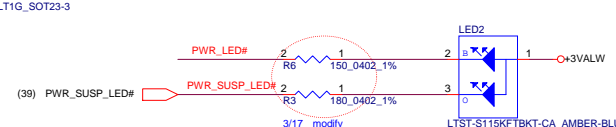
LED



Battery LED



Power LED



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Top Section: Power and ground planes. Includes components like C2133, C2120, C2118, C2119, C2114, C2115, C2116, C2117, C2118, C2119, C2120, C2121, C2122, C2123, C2124, C2125, C2126, C2127, C2128, C2129, C2130, C2131, C2132, C2133, C2134, C2135, C2136, C2137, C2138, C2139, C2140, C2141, C2142, C2143, C2144, C2145, C2146, C2147, C2148, C2149, C2150, C2151, C2152, C2153, C2154, C2155, C2156, C2157, C2158, C2159, C2160, C2161, C2162, C2163, C2164, C2165, C2166, C2167, C2168, C2169, C2170, C2171, C2172, C2173, C2174, C2175, C2176, C2177, C2178, C2179, C2180, C2181, C2182, C2183, C2184, C2185, C2186, C2187, C2188, C2189, C2190, C2191, C2192, C2193, C2194, C2195, C2196, C2197, C2198, C2199, C2200, C2201, C2202, C2203, C2204, C2205, C2206, C2207, C2208, C2209, C2210, C2211, C2212, C2213, C2214, C2215, C2216, C2217, C2218, C2219, C2220, C2221, C2222, C2223, C2224, C2225, C2226, C2227, C2228, C2229, C2230, C2231, C2232, C2233, C2234, C2235, C2236, C2237, C2238, C2239, C2240, C2241, C2242, C2243, C2244, C2245, C2246, C2247, C2248, C2249, C2250, C2251, C2252, C2253, C2254, C2255, C2256, C2257, C2258, C2259, C2260, C2261, C2262, C2263, C2264, C2265, C2266, C2267, C2268, C2269, C2270, C2271, C2272, C2273, C2274, C2275, C2276, C2277, C2278, C2279, C2280, C2281, C2282, C2283, C2284, C2285, C2286, C2287, C2288, C2289, C2290, C2291, C2292, C2293, C2294, C2295, C2296, C2297, C2298, C2299, C2300, C2301, C2302, C2303, C2304, C2305, C2306, C2307, C2308, C2309, C2310, C2311, C2312, C2313, C2314, C2315, C2316, C2317, C2318, C2319, C2320, C2321, C2322, C2323, C2324, C2325, C2326, C2327, C2328, C2329, C2330, C2331, C2332, C2333, C2334, C2335, C2336, C2337, C2338, C2339, C2340, C2341, C2342, C2343, C2344, C2345, C2346, C2347, C2348, C2349, C2350, C2351, C2352, C2353, C2354, C2355, C2356, C2357, C2358, C2359, C2360, C2361, C2362, C2363, C2364, C2365, C2366, C2367, C2368, C2369, C2370, C2371, C2372, C2373, C2374, C2375, C2376, C2377, C2378, C2379, C2380, C2381, C2382, C2383, C2384, C2385, C2386, C2387, C2388, C2389, C2390, C2391, C2392, C2393, C2394, C2395, C2396, C2397, C2398, C2399, C2400, C2401, C2402, C2403, C2404, C2405, C2406, C2407, C2408, C2409, C2410, C2411, C2412, C2413, C2414, C2415, C2416, C2417, C2418, C2419, C2420, C2421, C2422, C2423, C2424, C2425, C2426, C2427, C2428, C2429, C2430, C2431, C2432, C2433, C2434, C2435, C2436, C2437, C2438, C2439, C2440, C2441, C2442, C2443, C2444, C2445, C2446, C2447, C2448, C2449, C2450, C2451, C2452, C2453, C2454, C2455, C2456, C2457, C2458, C2459, C2460, C2461, C2462, C2463, C2464, C2465, C2466, C2467, C2468, C2469, C2470, C2471, C2472, C2473, C2474, C2475, C2476, C2477, C2478, C2479, C2480, C2481, C2482, C2483, C2484, C2485, C2486, C2487, C2488, C2489, C2490, C2491, C2492, C2493, C2494, C2495, C2496, C2497, C2498, C2499, C2500, C2501, C2502, C2503, C2504, C2505, C2506, C2507, C2508, C2509, C2510, C2511, C2512, C2513, C2514, C2515, C2516, C2517, C2518, C2519, C2520, C2521, C2522, C2523, C2524, C2525, C2526, C2527, C2528, C2529, C2530, C2531, C2532, C2533, C2534, C2535, C2536, C2537, C2538, C2539, C2540, C2541, C2542, C2543, C2544, C2545, C2546, C2547, C2548, C2549, C2550, C2551, C2552, C2553, C2554, C2555, C2556, C2557, C2558, C2559, C2560, C2561, C2562, C2563, C2564, C2565, C2566, C2567, C2568, C2569, C2570, C2571, C2572, C2573, C2574, C2575, C2576, C2577, C2578, C2579, C2580, C2581, C2582, C2583, C2584, C2585, C2586, C2587, C2588, C2589, C2590, C2591, C2592, C2593, C2594, C2595, C2596, C2597, C2598, C2599, C2600, C2601, C2602, C2603, C2604, C2605, C2606, C2607, C2608, C2609, C2610, C2611, C2612, C2613, C2614, C2615, C2616, C2617, C2618, C2619, C2620, C2621, C2622, C2623, C2624, C2625, C2626, C2627, C2628, C2629, C2630, C2631, C2632, C2633, C2634, C2635, C2636, C2637, C2638, C2639, C2640, C2641, C2642, C2643, C2644, C2645, C2646, C2647, C2648, C2649, C2650, C2651, C2652, C2653, C2654, C2655, C2656, C2657, C2658, C2659, C2660, C2661, C2662, C2663, C2664, C2665, C2666, C2667, C2668, C2669, C2670, C2671, C2672, C2673, C2674, C2675, C2676, C2677, C2678, C2679, C2680, C2681, C2682, C2683, C2684, C2685, C2686, C2687, C2688, C2689, C2690, C2691, C2692, C2693, C2694, C2695, C2696, C2697, C2698, C2699, C2700, C2701, C2702, C2703, C2704, C2705, C2706, C2707, C2708, C2709, C2710, C2711, C2712, C2713, C2714, C2715, C2716, C2717, C2718, C2719, C2720, C2721, C2722, C2723, C2724, C2725, C2726, C2727, C2728, C2729, C2730, C2731, C2732, C2733, C2734, C2735, C2736, C2737, C2738, C2739, C2740, C2741, C2742, C2743, C2744, C2745, C2746, C2747, C2748, C2749, C2750, C2751, C2752, C2753, C2754, C2755, C2756, C2757, C2758, C2759, C2760, C2761, C2762, C2763, C2764, C2765, C2766, C2767, C2768, C2769, C2770, C2771, C2772, C2773, C2774, C2775,

Digital MIC
MIC BOM upload by Audio Team

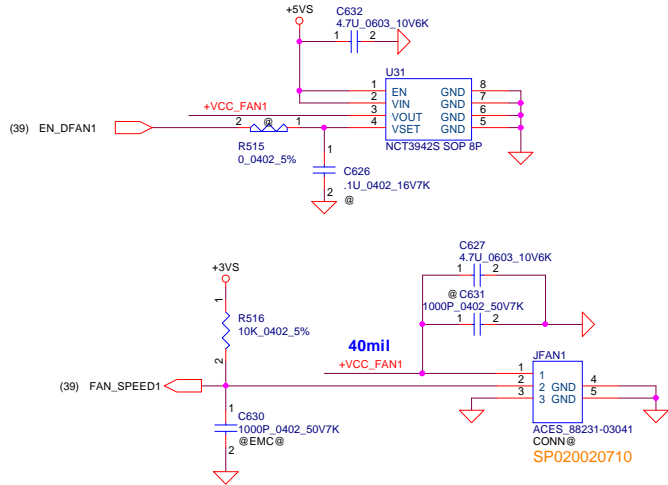
Headphone Out

Component Secret Data

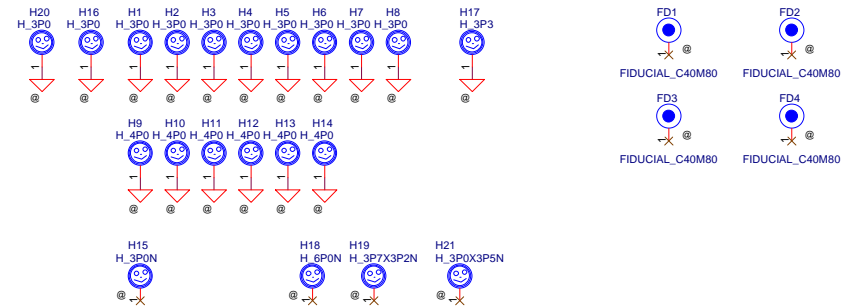
Deciphered Date	2016/12/31
Title: HD Audio Codec ALC283/ALC255 Colley	
Size: A4WAD M/B LA-C871P	
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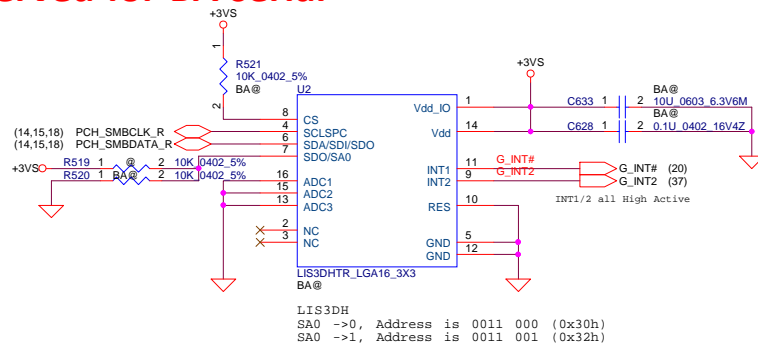
FAN1 Conn



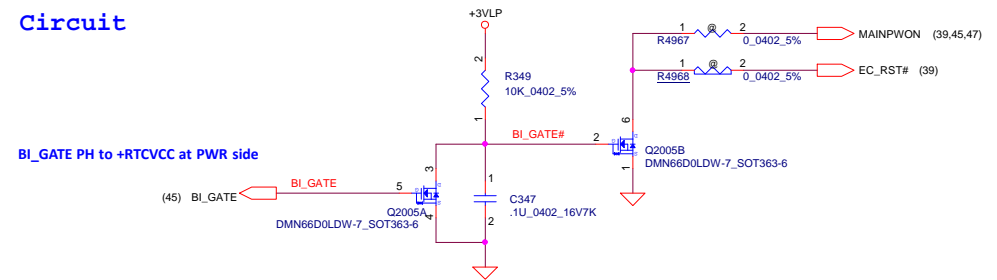
Screw Hole



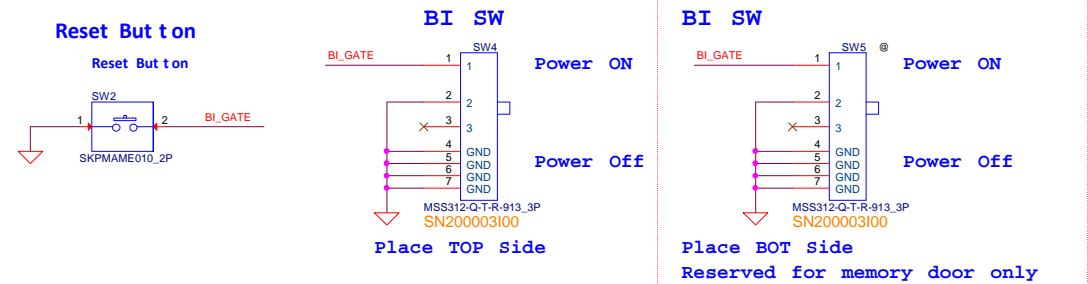
G-Sensor reserved for BA serial



Reset Circuit

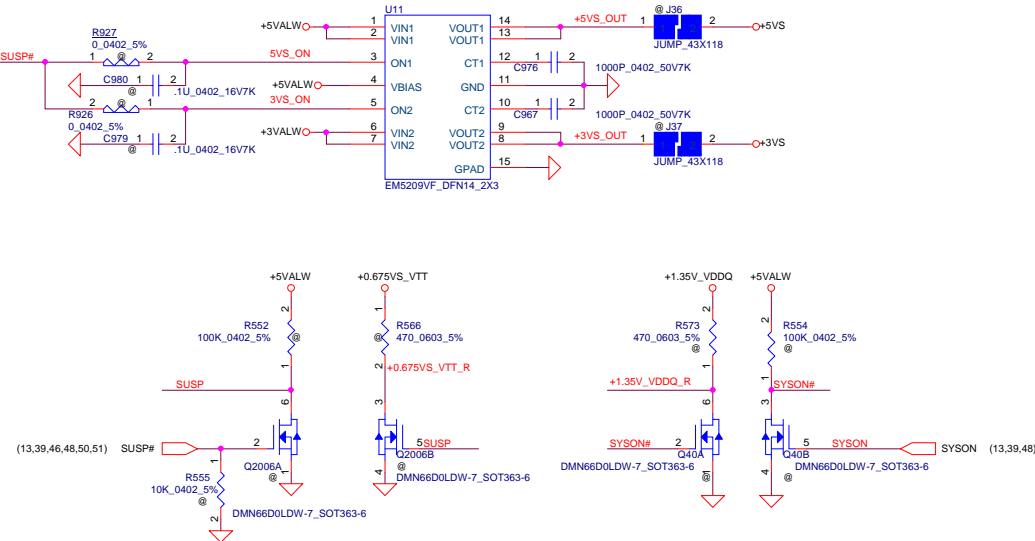


Debug SW

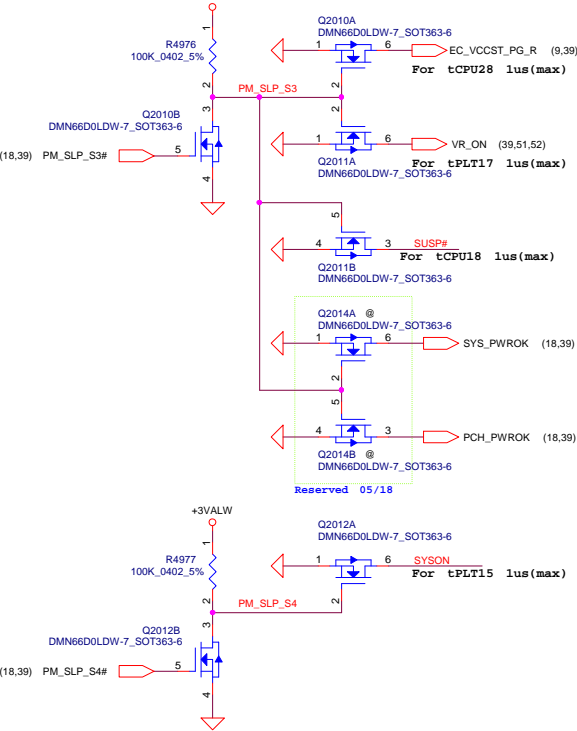


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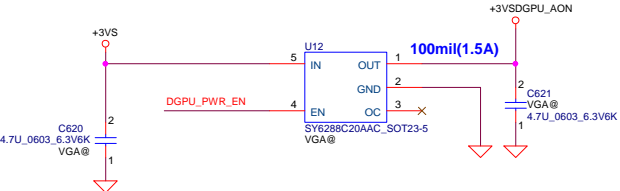
DC & VGA Interface



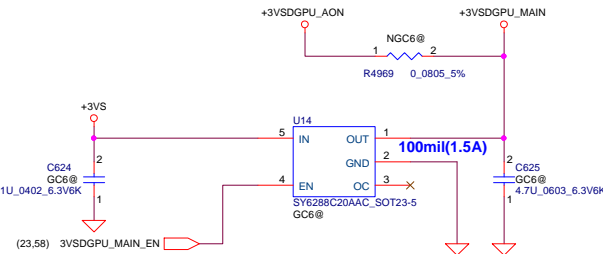
For Power Of f Sequence



+3VS to +3VSDGPU_AON for GPU



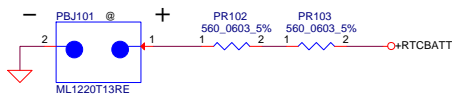
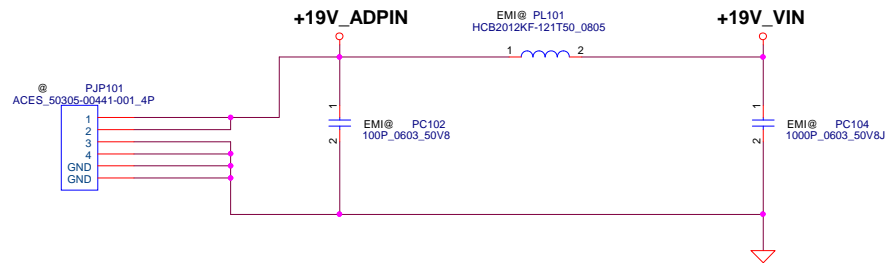
+3VS to +3VSDGPU_MAIN for GC6-2.0



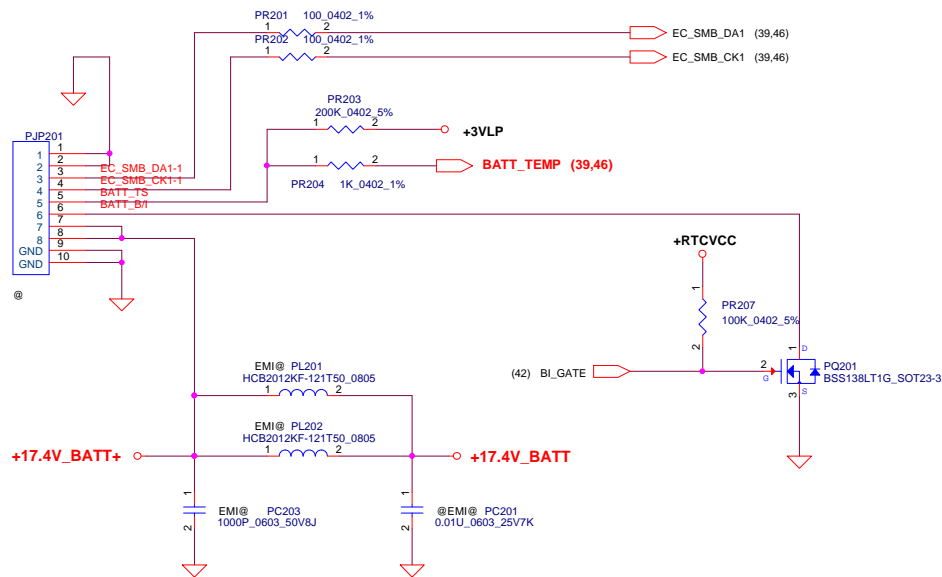
3VSDGPU_MAIN_EN From GPU



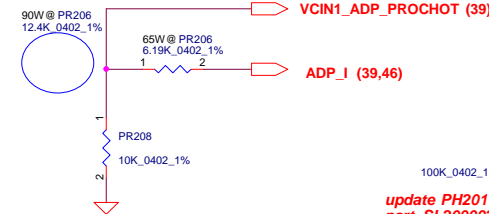
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				Document Number A4WAD M/B LA-C871P	1.0
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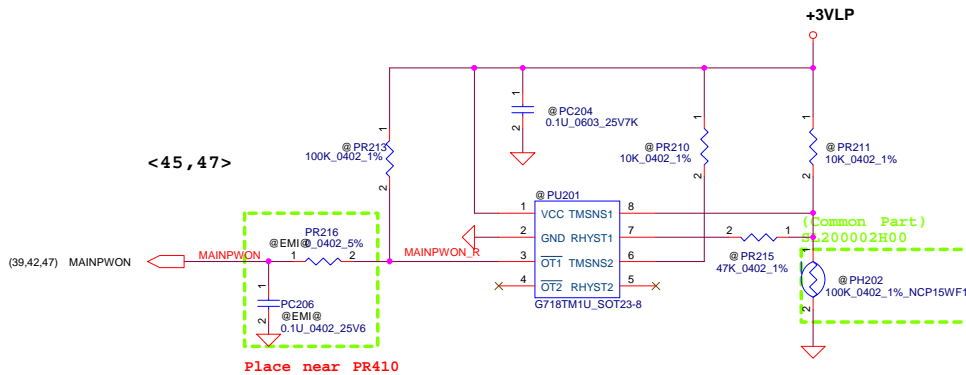
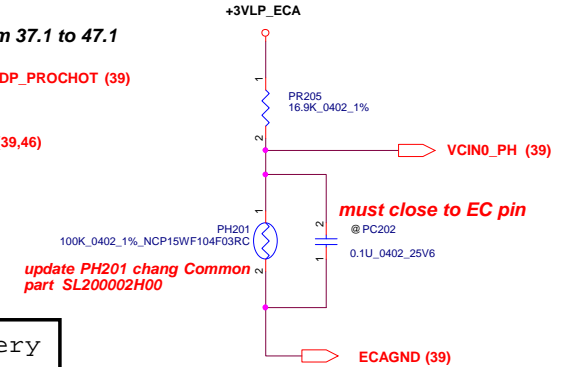


2013/07/23
change PC5 and PC6 function field from 37.1 to 47.1



For KB9022 sense 20mΩ	Active	Recovery
65W PR206 6.19K ohm	84.5W, 0.54V	65W, 0.42V
90W PR206 12.4K ohm	117W, 0.54V	90W, 0.42V

PH1 under CPU bottom side :
CPU thermal protection at 93 ±3 degree C
Recovery at 56 ±3 degree C

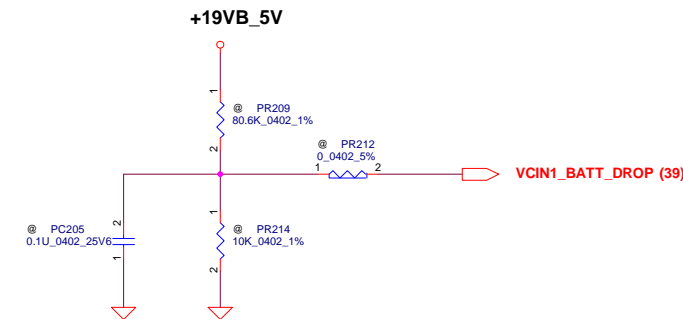


For 65W adapter====>action 84.5W, recovery 65W
65W:
 $I_{ada}=0\sim 3.42A$ ($65W/19v=3.42A$)
 $ADP_I=20*I_{ada}*R_{sense}$
 $=20*3.42*0.01=0.6842V$
 $VCIN1_PROCHOT=0.6842*10/(10+x)=0.42V$
 $PR206=x=6.291k\ ohm$

84.5W:
 $I_{ada}=0\sim 4.447A$ ($84.5W/19v=4.447A$)
 $ADP_I=20*I_{ada}*R_{sense}$
 $=20*4.447*0.01=0.8895V$
 $VCIN1_PROCHOT=0.8895*10/(10+x)=0.55V$
 $PR206=x=6.17k\ ohm$

For 90W adapter====>action 117W, recovery 90W
90W:
 $I_{ada}=0\sim 4.737A$ ($90W/19v=4.737A$)
 $ADP_I=20*I_{ada}*R_{sense}$
 $=20*4.737*0.01=0.9474V$
 $VCIN1_PROCHOT=0.9474*10/(10+x)=0.42V$
 $PR206=x=12.56k\ ohm$

117W:
 $I_{ada}=0\sim 6.158A$ ($117W/19v=6.158A$)
 $ADP_I=20*I_{ada}*R_{sense}$
 $=20*6.158*0.01=1.232V$
 $VCIN1_PROCHOT=1.232*10/(10+x)=0.55V$
 $PR206=x=12.39k\ ohm$



2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

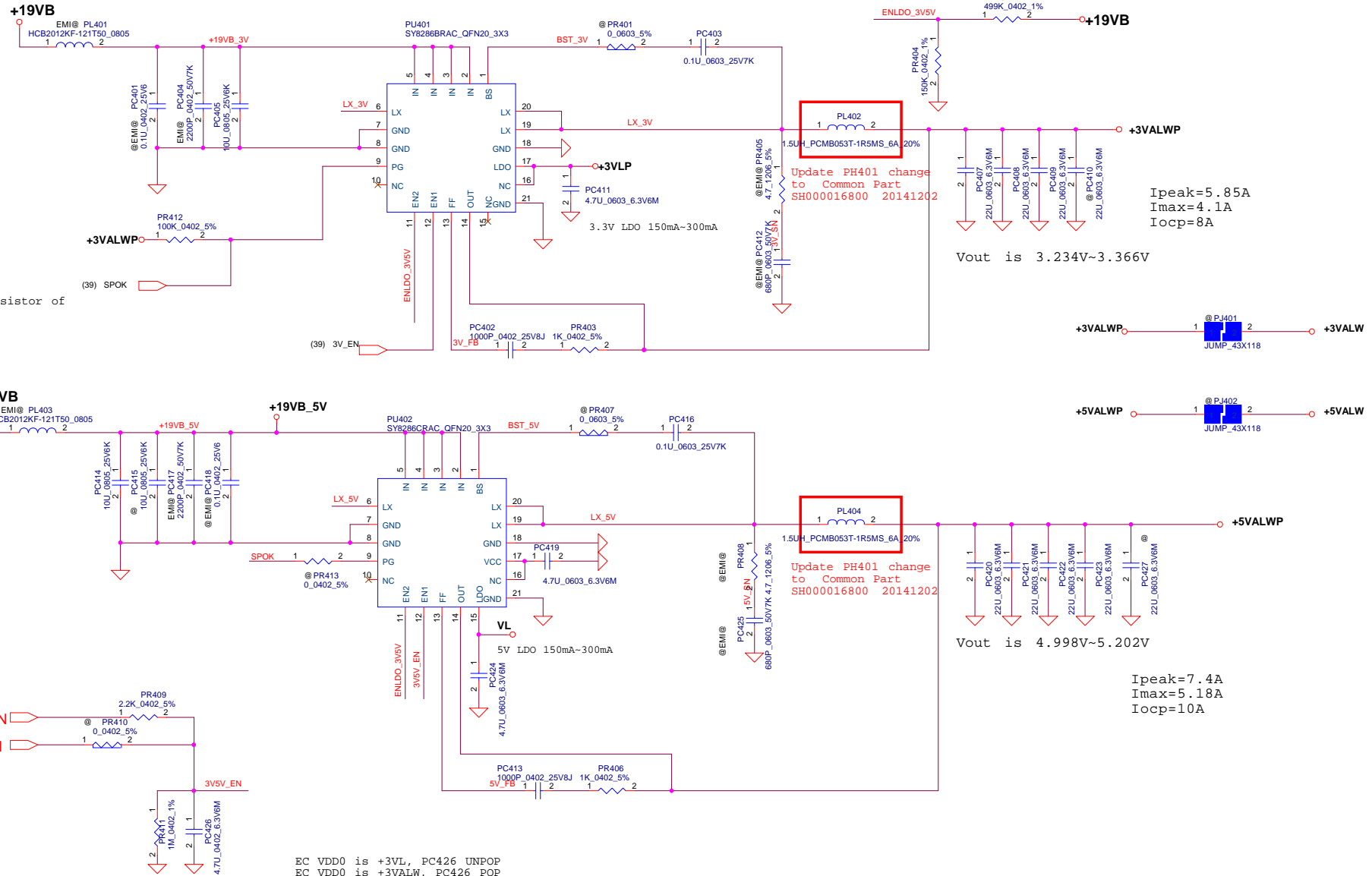
VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50k if Battery is 2-cell NVDC design
B+=6V

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Module model information

SY8208B_V2.mdd

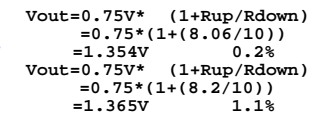
SY8208C_V2.mdd



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				Rev	1.0

RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer

```
0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A
```



Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
VFB=0.75V, Vout=1.3545V
MOSFET footprint: SIS412DN

```

Mode   Level   +0.675VSP   VTTREF_1.35V
S5     L       off      off
S3     L       off      on
S0     H       on       on

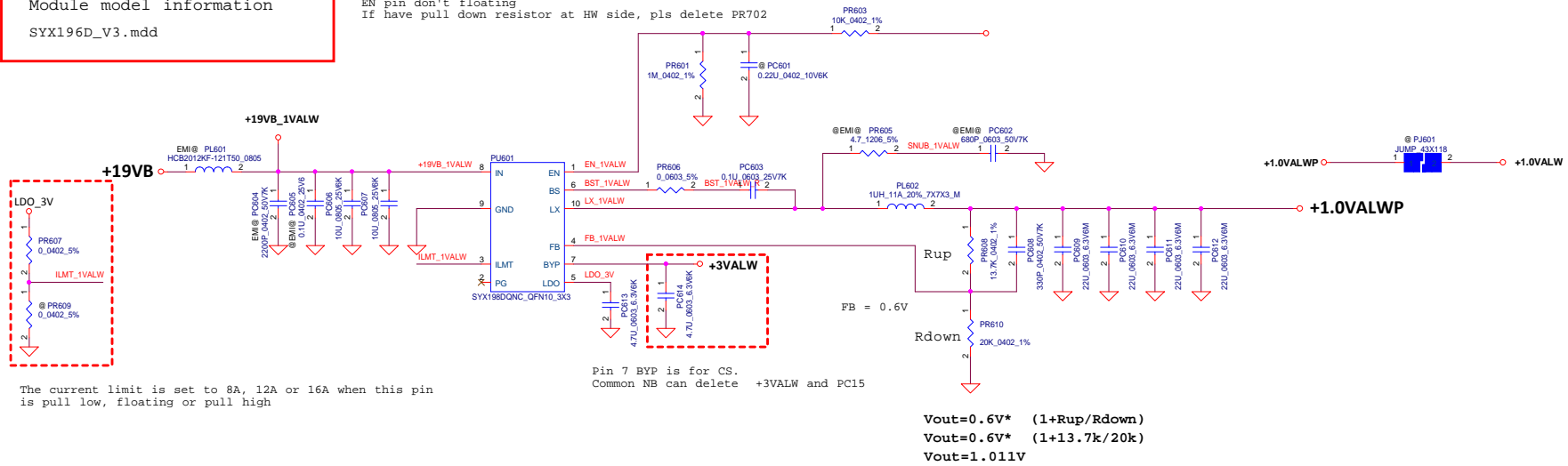
Note: S3 - sleep ; S5 - power off

```

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SYX196D_V3.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



```
Function Field :
VCCEDPIO : IC-35.21 , others - 35.22
VCCEDRAM : IC-35.25 , others - 35.26
```

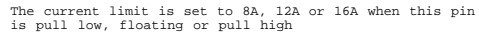
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						Size	Document Number		Rev
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SYX196D_V3.mdd

Timing diagram for the 1-wire protocol. The diagram shows the relationship between the **VR_ON** signal (pin 39, 43, 52), the **SUSP#** signal (pin 13, 39, 43, 46, 48, 50), and the **EN_1VS_VCCIO** signal (pin 1VS_VCCIO). The **SUSP#** signal is shown with a delay measurement point. The delay is measured from the rising edge of **SUSP#** to the rising edge of **EN_1VS_VCCIO**. The delay is labeled as "check delay time with HM".

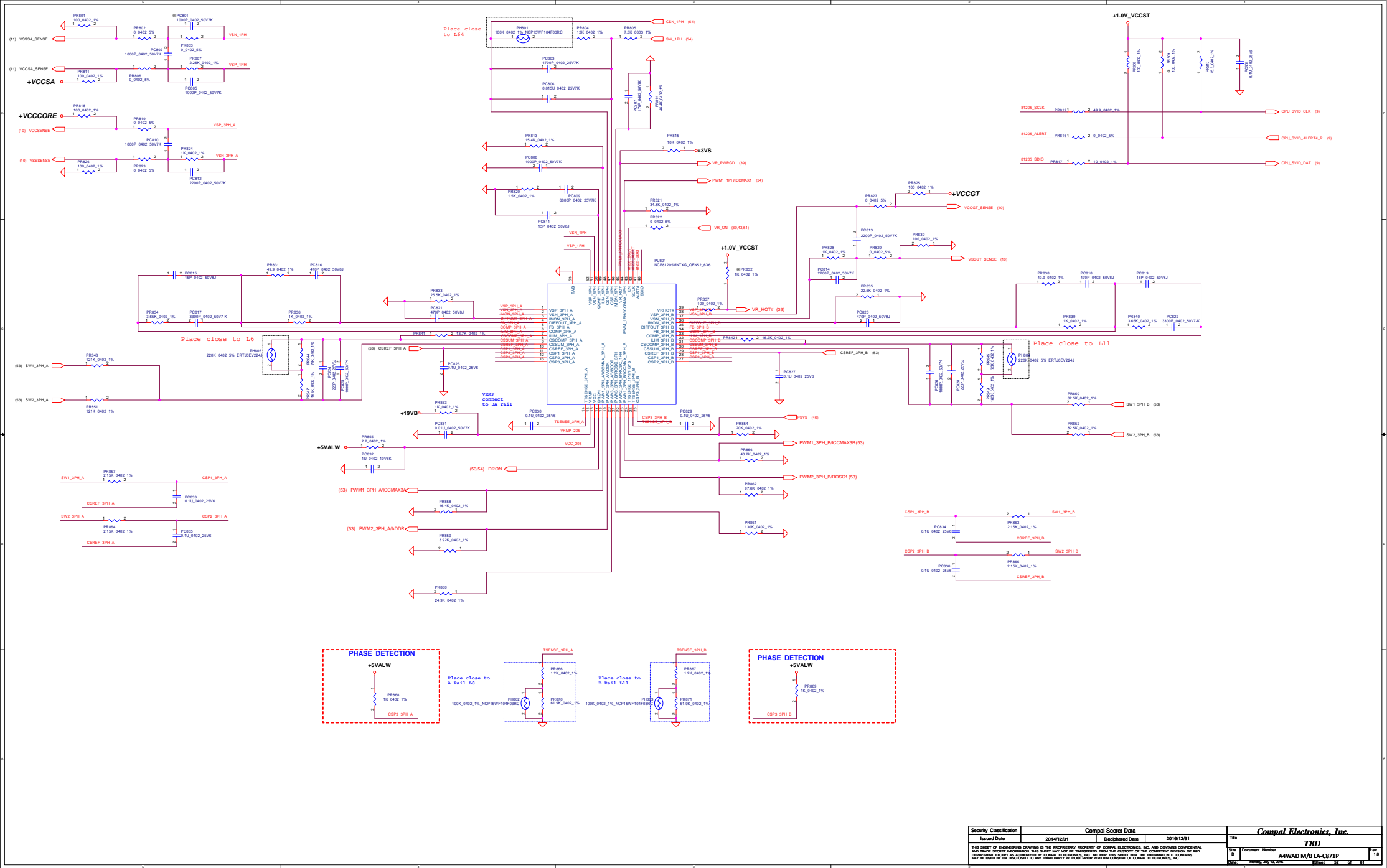
The diagram includes a resistor network for the delay measurement. The network consists of a 1K 0.402 5% resistor (PR95) and a 1M 0.402 5% resistor (PR94). The delay is measured across the 1K resistor. The delay is labeled as "check delay time with HM".

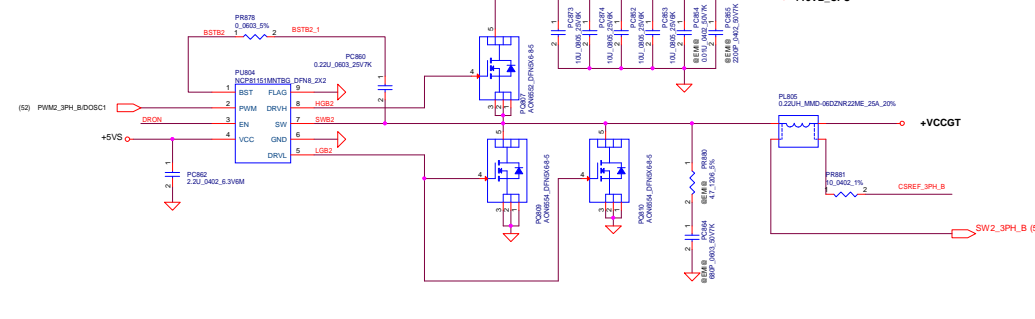
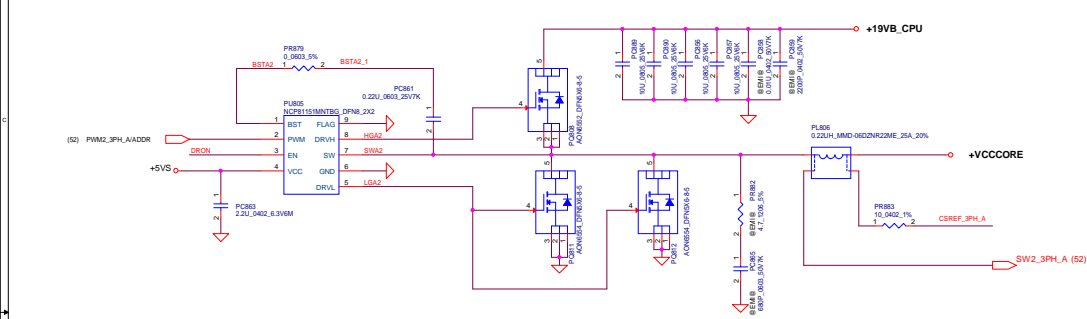
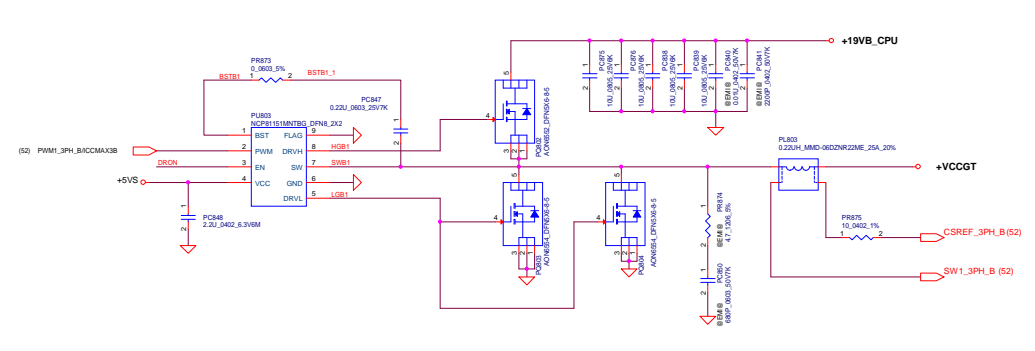
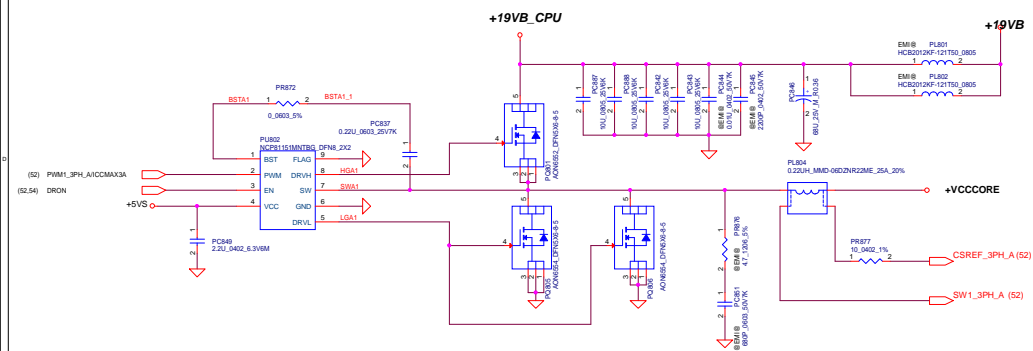
The diagram also shows a 0.1uF capacitor connected to the **EN_1VS_VCCIO** signal. The capacitor is connected to ground. The capacitor is labeled as "0.1uF 0.125V".



+VCCIO **VFB=0.6V** **Ipeak=5.35A**
 Vout=0.6V* (1+Rup/Rdown) **Iocp=6A**
 Vout=0.6V* (1+11.8k/20k)
 Vout=0.95V

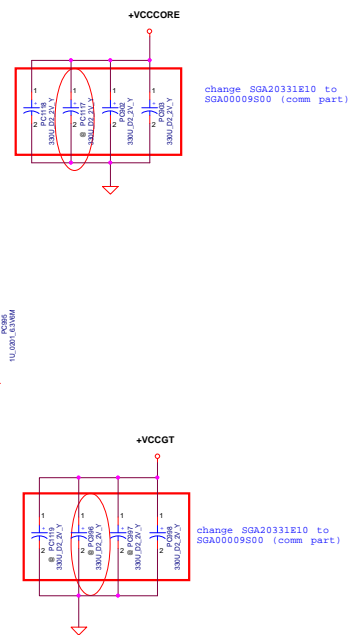
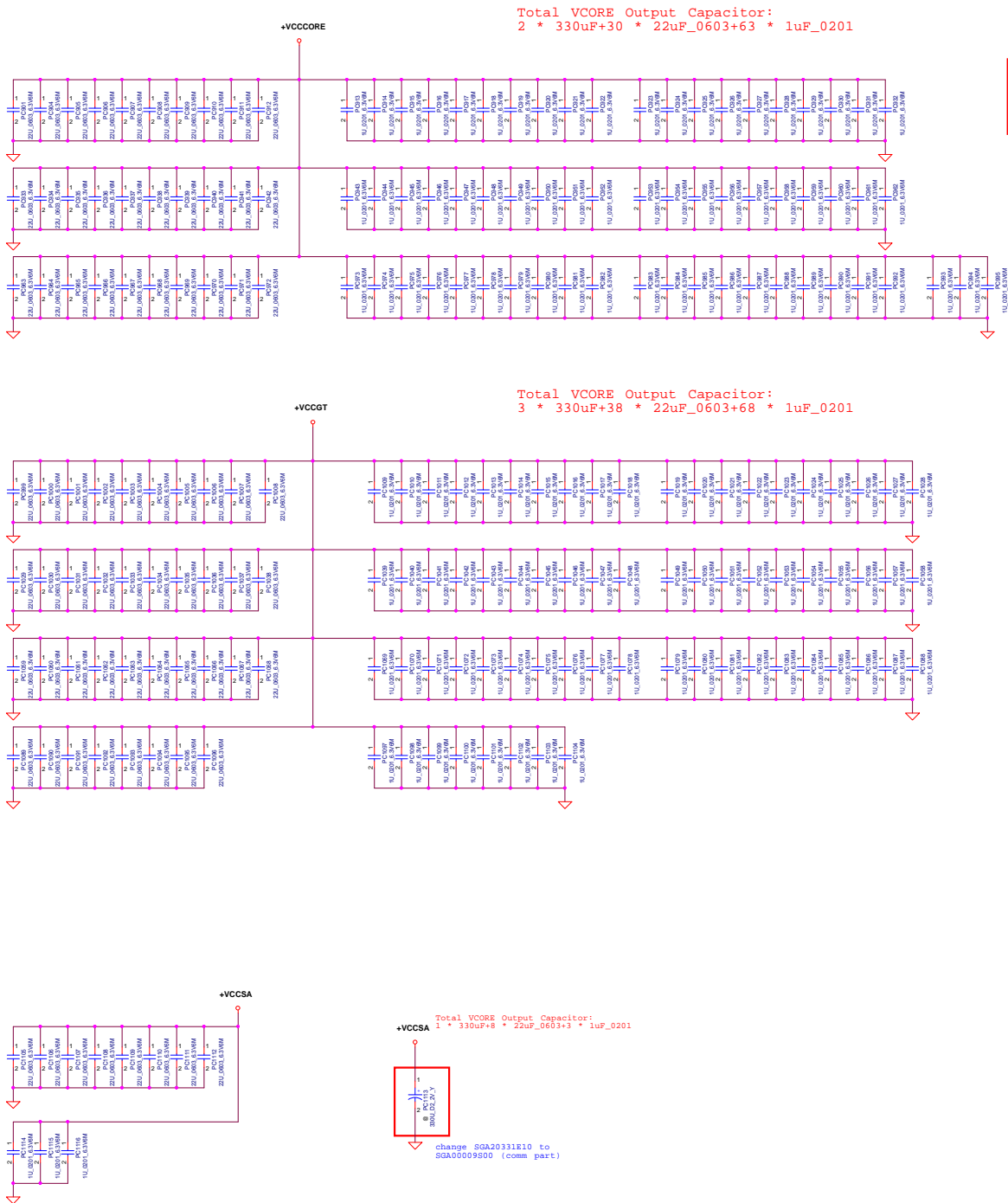
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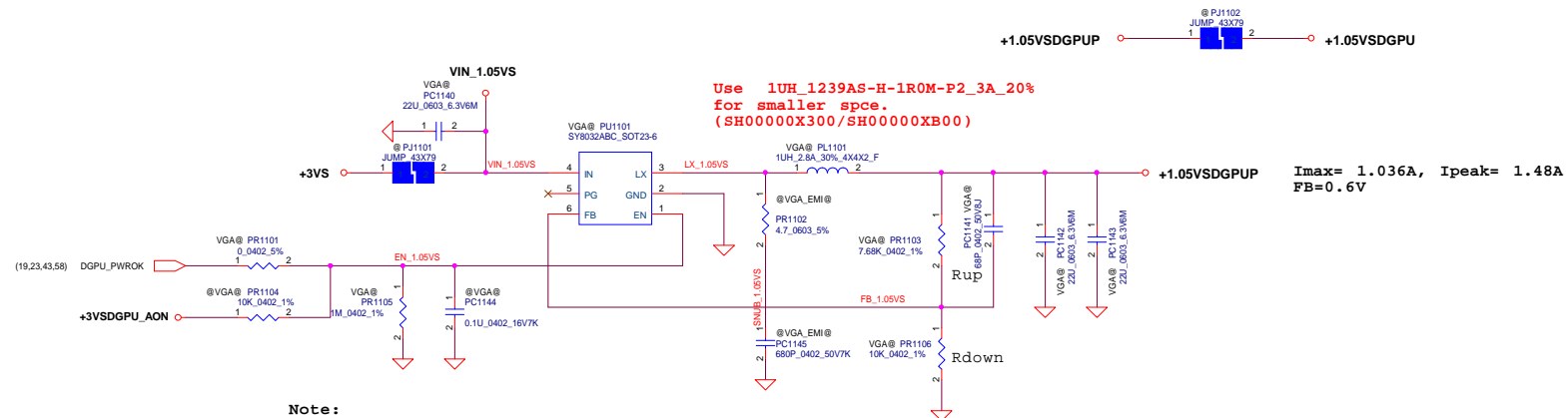


+VCCCORE
 TDC 64A
 Peak Current 60A
 OCP current 76A
 Load line mV/A
 FSW=400kHz
 DCR 0.98mohm +/-5%
 TYP
 H/S Rds(on) : 6.7mohm , 8.5mohm
 L/S Rds(on) : 3mohm , 3.7mohm

+VCCGT
 TDC 49A
 Peak Current 55A
 OCP current 61A
 Load line mV/A
 FSW=400kHz
 DCR 0.98mohm +/-5%
 TYP
 H/S Rds(on) : 6.7mohm , 8.5mohm
 L/S Rds(on) : 3mohm , 3.7mohm



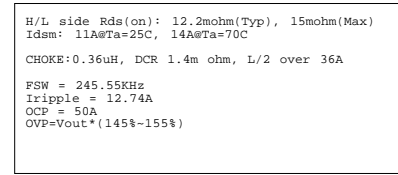
Module model information
SY8032_V2.mdd



$$\begin{aligned} V_{out} &= 0.6V * (1 + R_{up}/R_{down}) \\ &=> 0.6V * (1 + (7.68/10)) = 1.061 \quad (1.01\%) \\ &=> 0.6V * (1 + (7.87/10)) = 1.072 \quad (2.1\%) \end{aligned}$$

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EN High Threshold = 1.6V



Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	ACIN can't boot	ACDET pin below 2.4V. It must above 2.4V.	02	46	1. Change PR313 59K to 66.5K	4/6	DVT
02	X1 Code	X1 code changed to AP code.	02	52	1. Change PC824,PC828 S CER CAP 220P 25V J NPO 0402	4/6	DVT
03	Design Change.	CPU CORE transient noise meets spec.	02	55	1. Delete PC1119,PC997 S POLY C 330U 2V Y ESR9M H1.9	4/6	DVT
04	Design Change.	For EMI Test	02	46	1. Add PL302 S COIL 1UH +-30% 2.8A 4X4X2 FERRITE	4/6	DVT
05	The sequence of VGA CORE is't correct	For VGA CORE Sequence	02	58	1.Change PR1202 10K ohm to 20k ohm 2. Change PR1206 0 ohm to 20k ohm 3. Add PC1209 S CER CAP .1U 16V K X7R 0402	4/6	DVT
06	Design Change.	For VGA ILIMIT	02	58	1. Change PR1214 11.8K to 13K	4/6	DVT
07	Design Change.	For meeting CPU Thermal criteria	02	52	1. Change PR866,PR867 909ohm to 1.2Kohm	4/6	DVT
08	Design Change.	For S5 mode, charger current charge	02	46	1.Add PR320 for power source 3VALWP to 3VLP. 2.Add PR239 for reserved 5VALWP	5/15	PVT
09	Design Change.	Changing VCCIO solution for power efficiency.	02	51	1. Change SY196D to SY198D	5/16	PVT
10	Design Change.	To decrease part count,no EMI concerned	02	47	1. Change PR401,PR407 to short pad	5/16	PVT
11	Design Change.	To decrease part count,no EMI concerned	02	53	1. Change PR1224,PR1201,PR1217,PR1219,PR1204 to short pad	5/16	PVT
12	Design Change.	Reserve for Intel solution	02	44	1. Change PR101 to 0 ohm	5/16	PVT
13	Design Change.	For meet DFB	02	46	1. Delete PJ301		
14	Design Change.		02	50			
15	Design Change.		02	45			
16	Design Change.		02	48			
17	Design Change.		02	50			

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Item	Page	Title	Date	Solution Description		Phase	Rev.
1	6	CMC	3/17	Change XDP to CMC	Change JXDP1 CIS symbol to CMC CIS Symbol(JPCMC1) Rerouting RPC1, RPC2, RPC3, RC56 Del CC1,CC2,CC70,JXDP1,RC12,RC14, RC16,RC18,RC48,RC49,RC50,RC51, RC53,RC54,RC55,RC7,RC9,RPH10 Add JPCMC1,RC59	DVT	0.2
2	9,18,19	CPU,PCH	3/17	change XDP to CMC CONN, reserved test point	Add T3820,T3821,T3822,T3823	DVT	0.2
3	7	CPU	3/17	549401_549401_SKL_H_S_Plat_SMI_WP_Rev0_93	UC1.AU5 UC1.AR8 <DDR_ALERT#> Not used at DDR3L. Tied to GND.	DVT	0.2
4	17	PCH	3/17	Reserved path for TP_INT	Add RH148 0R @	DVT	0.2
5	17	SPI	3/17	546765_546765_2015WW09_Skylake_MOW_Rev_1_0	Change RH28 to @	DVT	0.2
6	31	HDMI	3/17	Reduce unuse part	Del R4962,R4963,R4975	DVT	0.2
7	34	LAN	3/17	Reserved path for +3V_LAN	Add R4984 @ 0_0805_5%	DVT	0.2
8	36	WLAN (M.2)	3/17	follow A4WAS (Reqruie from Acer) Separate M.2 pin32 and 46 for Intel WLAN 3165	Change "E51RXD_P80CLK_R" to JNGFF1.46	DVT	0.2
9	39	Board ID	3/17	Board ID change to DVT	Change R4903 from 0_0402_5% to 12K_0402_5%	DVT	0.2
10	40	LED	3/17	Follow A4WAD LED Light adjust report	change R1 to 750_0402_1% change R2 to 820_0402_1% change R3 to 180_0402_1% change R6 to 150_0402_1%	DVT	0.2
11	42	BI SW	3/17	Reserved for memory door on D-Cover, place BOT Side	Add SW5 @	DVT	0.2
12	9	PCH	3/20	follow PCH EDS Rev1.5 USB2_ID,USB_VBUSSENSE PD	Add RH149,RH150 1k_0402_5% to GND	DVT	0.2
13	39	EC	3/20	Reserved TPT PU RES	Del R4908,R4910	DVT	0.2
14	39	LID	3/30	EC doesn't internal PU	Change R618 to stuf f	DVT	0.2
15	20	G Sensor	4/1	Reserved	Reserved RH151 PD 100K @ to "G_INT#"	DVT	0.2
16	19	X'TAL	4/8	Change Common part	Change YH1 to S CRYSTAL 32.768KHZ CM7V-T1A9.0PF20PPM	DVT	0.2
17	19	X'TAL	4/8	Follow X'TAL test report	Change CH13 to 10p , CH14 to 8.2p	DVT	0.2
18	19	X'TAL	4/8	Follow X'TAL test report	Change CH11,CH12 to 15p	DVT	0.2
19	18	SMBUS	4/13	Follow INTEL PDG	Change RPH8,RPH9 to 2.2K_0804_8P4R_5%	DVT	0.2
20	41	PC BEEP	4/13	Colay PC_BEEP to EC	Change R2138 to stuf f	DVT	0.2
21	23	NV SMBus	4/13A	Follow INTEL PDG,already conf ir m with NV D A	Change R2000,R2001 to 4.7K_0402_1%	DVT	0.2
22	21	PCH	5/18	Recommend to follow intel PDG decoupling requirement.	add CH54 1u_0402 for UH1.W15 "+3VALW_DSW" change UH1.V28 & AC17 connected to "+1.0VALW_MPHY"	PVT	0.3

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